SERVICING HANDBOOK

Volume 1

4920M

Alternating Voltage Measurement Standard

Datron Instruments Ltd. 52 Hurricane Way, Norwich Airport, Norwich, Norfolk NR6 6JB, England.
Documentation Part No. 850262-1

MOD LEVEL 3

SERVICING HANDBOOK

for

THE DATRON 4920M

ALTERNATING VOLTAGE MEASUREMENT STANDARD

Volume 1

Calibration and Servicing Information

Technical Descriptions

For any assistance contact your nearest Datron Sales and Service center.
Addresses can be found at the back of this handbook.

850262

Issue 1 (July 1990)

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DANGER
HIGH VOLTAGE

THIS INSTRUMENT IS CAPABLE OF DELIVERING
A LETHAL ELECTRIC SHOCK !
when connected to a high voltage source

Input plugs carry the Full Input Voltage

THIS CAN KILL !

Overvoltage can damage your instrument !

Unless **you** are **sure** that it is **safe** to do so,
DO NOT TOUCH
any **terminals** connected to the **inputs**

DANGER

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SECTION 1 CALIBRATION

1.1 Routine Calibration

The main features of the routine calibration facilities are described in Section 4 of the User's Handbook. Routine calibration procedures are detailed in Section 8 of the User's Handbook

1.2 Internal Access

The high accuracy of the instrument demands that its internal environment remains undisturbed. This implies that a Routine or 'Special' (Maintenance) calibration must follow any internal access, such as battery-changing, fault-finding or replacement of PCBs. Refer to *Section 4*.

1.3 Remote Calibration via the IEEE 488 Interface

The 4920M is designed as an Alternating Voltage Measurement Standard, its levels of accuracy demanding that it be calibrated against primary laboratory standards. The traceabilities of such standards are derived through physical devices which are as yet not remotely programmable, although the calibration facilities of the 4920M are included in its conformity to IEEE 488.2, against a time when such standards are available on the bus.

It is possible to characterize an individual calibration standard such as the Datron model 4708 at the levels required to calibrate a 4920M to its specification. The Datron 'Portocal' system can be programmed to perform these tasks automatically providing a 4708 in the system is adequately characterized. If the 4920M is not required to operate at its full specification, a regular 4708 in a remote system (e.g. Portocal) can easily be programmed to perform this task.

1.4 Special Calibration

The main purpose of this section is to describe and detail procedures for five Special Calibrations which may be required under certain conditions. These are listed on the **SPCL** menu, which is accessed via the **CAL** menu. They are:

WLIn	Internal calibration of the linearity of the 3V Wideband range. External input must not be connected. *Refer to paras 1.4.2.*
Filt	Calibration of the internal 10Hz filter. *Refer to paras 1.4.3.*
Flat	Flatness calibration all ranges. *Refer to paras 1.4.4.*
ALIn	Calibration of the Normal Band linearity on the 10V High Accuracy ACV range. *Refer to paras 1.4.5.*
ClrNv	Clearing a section of the non-volatile RAM. *Refer to paras 1.4.6.*

Movement between the special calibration menus is illustrated in detail overleaf.

1.4 Special Calibration (Contd.)

1.4.1 Entry into the SPCL Menu

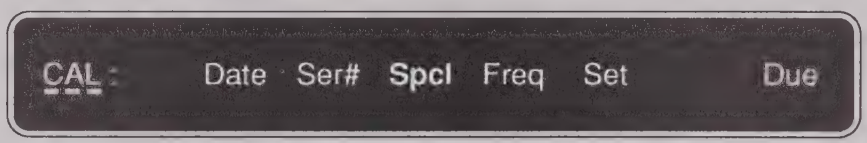
CAL Group of Menus

A description of the User Interface is given in Section 3 of the User's Handbook for the main functions. If you are unfamiliar with the front panel controls, you should complete the quick tour which starts on Page 3-5.
To give an overall view, movement among the SPCL group of menus is described by the diagram on the opposite page.

Access to Special Calibration

To carry out any of the special calibrations it is first necessary to enter the **SPCL** menu via the **CAL** menu. The **CAL** menu is protected, and once active, the **Caltrig** key is enabled. For these reasons, users are referred to the '**Preparation**' procedure detailed on page 8-5 of the User's handbook. Further details of the calibration facilities are described in Section 4 of the User's Handbook, beginning on page 4-20; the **CAL** menu description starts on page 4-21.

The CAL Menu

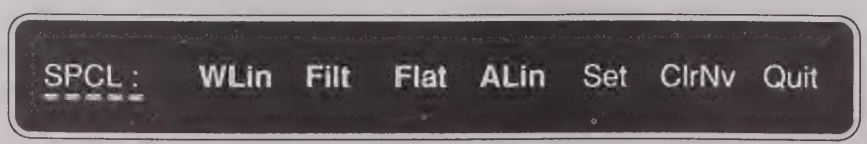


Once the **CAL** menu is active, pressing the **Spcl** soft key transfers via a warning 'Check' menu.

Check Menu

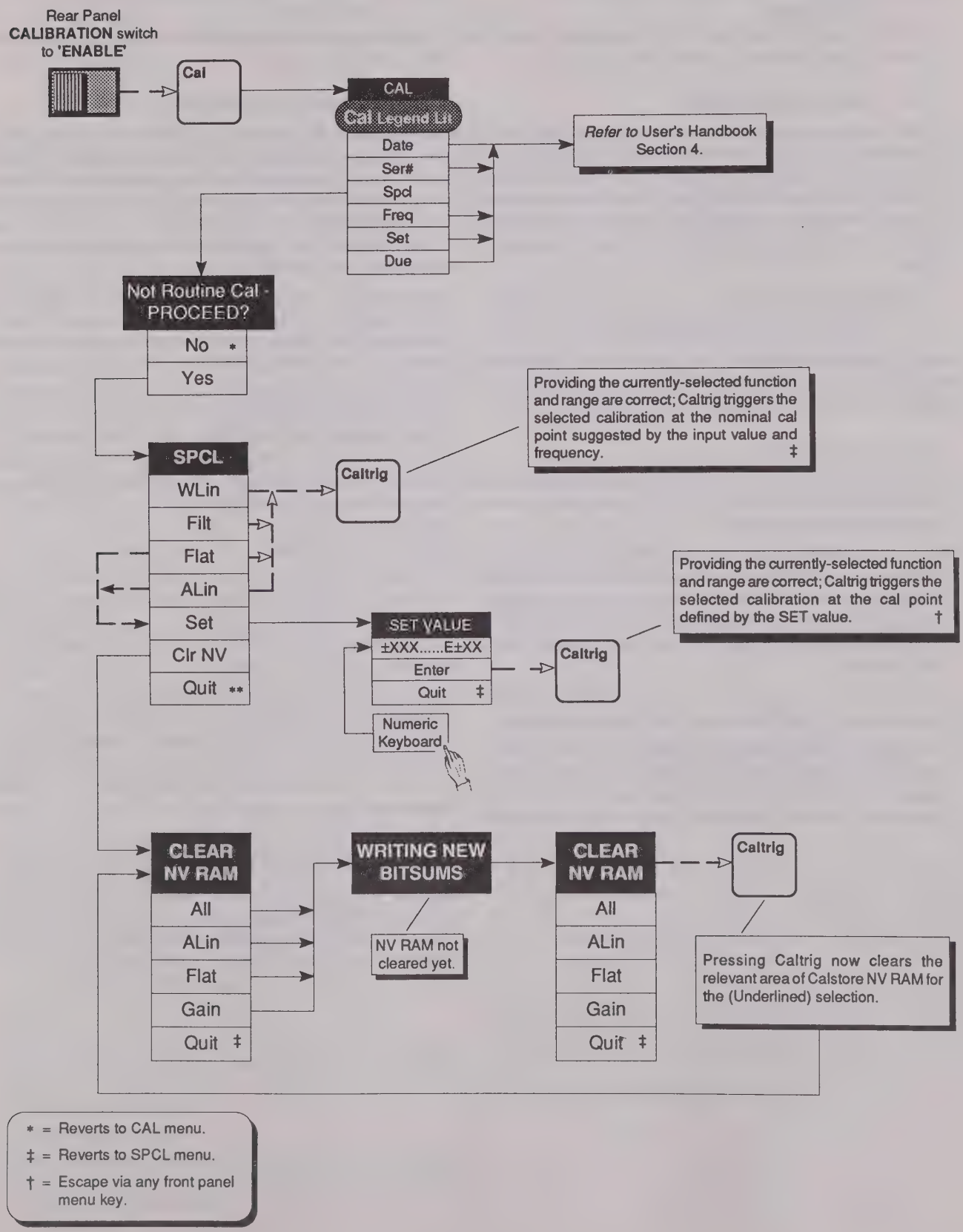
Pressing the **Yes** soft key transfers directly to the **SPCL** menu.

The SPCL Menu



The special calibrations highlighted in the above menu diagram are described in the following sub-sections 1.4.2 to 1.4.5. Sub-section 1.4.6 deals with clearance of the non-volatile RAM calibration memory.

SPCL Group of Menus - Overall View



1.4.4.5 Equipment Required for Flatness Calibration

The following equipment is required:

Equipment Type	Range	Accuracy [1][2]
DC Voltage Calibrator [3] † e.g. Datron Model 4708 with Option 10	Voltage: 100mV to 1000V Resolution: 1ppm	±4ppm
AC Voltage Calibrator/ **High Resolution AC Voltage Source**[3] e.g. Datron Model 4708 with Option 20	Voltage: 300mV to 1000V Frequency: 10Hz to 1MHz Resolution: 1ppm	1V to 3V: ±210ppm at 10Hz ±100ppm at 1kHz ±5ppm short-term stability
Wideband AC Voltage Source * e.g. Wavetek Model 178	Voltage: 1V to 3V Frequency: 10Hz to 20MHz	±50ppm short-term stability
Wideband Amplifier *	Voltage: 1V to 3V Frequency: 10Hz to 20MHz Gain: 1 approx.	±25ppm short-term stability
Thermal Voltage Converters e.g. Holt Model 11, and Ballantine Model 1396	Voltage: 300mV to 1000V Frequency: DC to 20MHz	To best NIST uncertainties
DC Nanovoltmeter e.g. EM Model N2a or Keithley Model 181	±100nV to ±10mV	Better than 2% of range
DC nV Source e.g. EM Model S6	10mV	±1ppm short-term stability

* Required for flatness calibration of the WBV 3V range only - see Fig. 1.4.2.

† Required for linearity calibration of the ACV ranges only -see Fig. 1.4.3.

[1] Absolute accuracy (traceable to National Standards, and inclusive of National Standards uncertainties).

[2] Provides a 95% confidence level of achieving a 4:1 calibration ratio except where 'state-of-the-art' limitations apply.

[3] This equipment can be part of a single AC/DC unit. e.g. a Datron 4708 multifunction calibrator with Options 10 and 20.

1.4.4.6 Preparation

1. Before operating any of the calibration equipment, familiarize yourself with the equipment by reading the appropriate operating manuals. In particular, note the electrical and mechanical handling procedures required to maintain the calibration of the thermal voltage converters.
2. **Note any safety precautions which are necessary to prevent electrical shock from the equipment.**
3. Set up the equipment in a stable environment at 23°C±1°C, power it on and allow it to stabilize for an appropriate period of time. The 4920M should be allowed to stabilize for a minimum of 2 hours after it is powered on.
4. On the 4920M, select the **TEST** menu by pressing the front-panel **Test** key. Select the **Oper** (Operational Test) menu option.

   Allow the operational self-test to run to completion, at which point the instrument dot-matrix display should show the word **COMPLETED**. If at any point during the operational self-test the 4920M displays the words **OPER FAIL** (Operational Test Failure) the unit probably has a fault. In this case refer to Section 2 before proceeding.
5. Set the rear-panel **CALIBRATION** switch to the **ENABLE** position.
6. Press the front-panel **Cal** key to open the **CAL** menu.
7. From the **CAL** menu, select **Spcl** to open the **SPCL** menu.

1.4.4.7 ACV Ranges and WBV 1V Range - Flatness Calibration setup

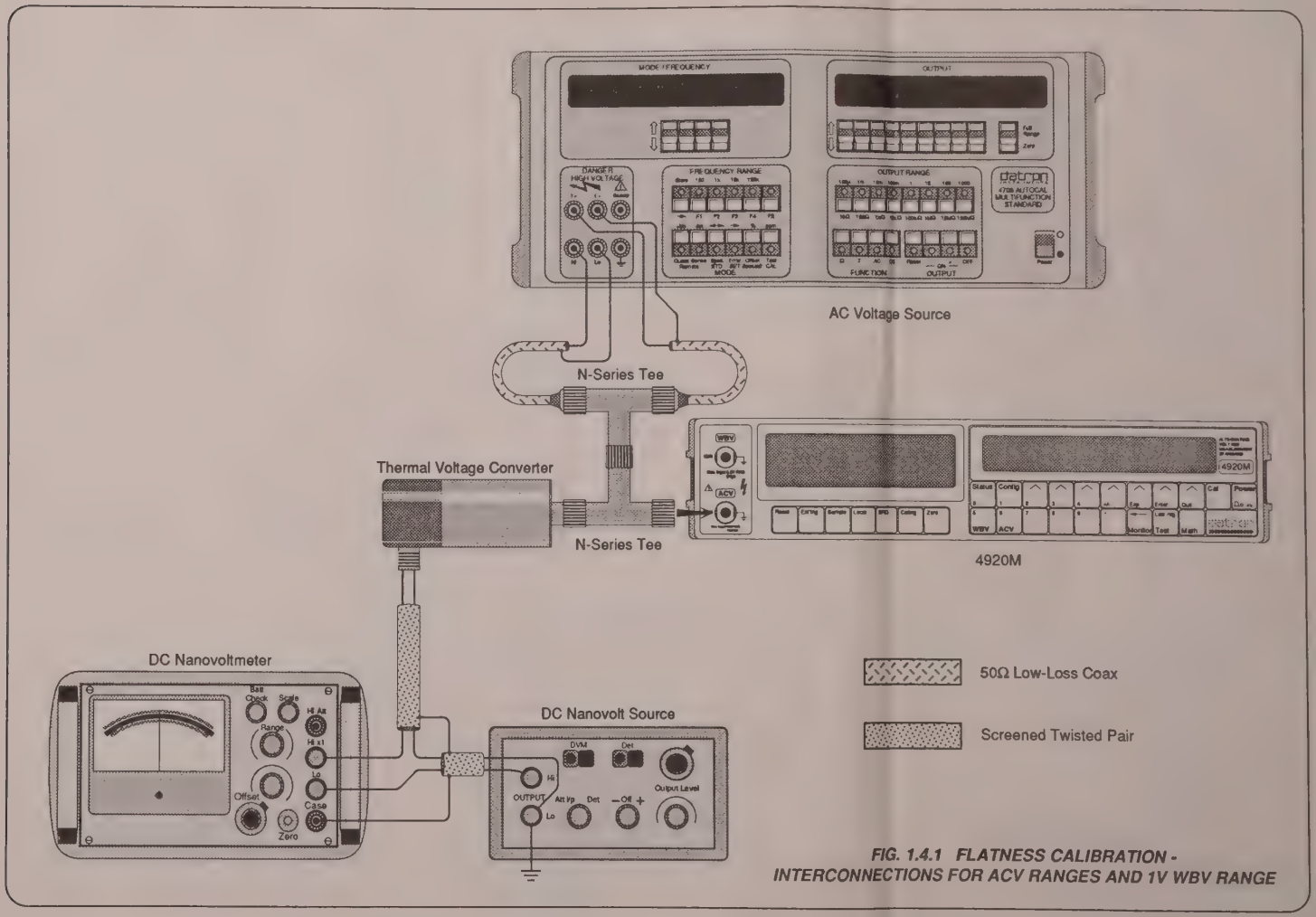


FIG. 1.4.1 FLATNESS CALIBRATION - INTERCONNECTIONS FOR ACV RANGES AND 1V WBV RANGE

1.4.4.8 ACV Ranges and WBV 1V Range - Flatness Calibration Procedure

Note 1
For flatness calibration of any currently selected range:
Vc is the required calibration voltage;
Fc is the recommended frequency.

Note 2. TVC Calibration
In the following procedures, the Thermal Voltage Converter is used to allow the 1kHz signal level to be remembered by the setting of the DC Nanovolt Source which nulls the TVC DC output. The flatness error for a particular Fc (relative to 1kHz) is measured by applying Fc to the TVC and adjusting the ACV source output to give the same null.

For this process to be accurate, it is necessary to account for the flatness of the TVC at Fc relative to 1kHz. The flatness figures are usually available in tabular form on the most-recent calibration certificate for the TVC in use.

The most usual method of recording the TVC response, at its calibrated frequencies, is to give a correction figure which is the incremental difference between the AC and DC inputs which produce the same output.

The difference is usually expressed in ppm with a polarity sign. On most calibration certificates, a 'plus' sign indicates that a higher value of ACV input is necessary to produce the same output as a DCV input.

In the procedure we do not compare ACV with DCV. For flatness calibration we need to compare the ACV value at Fc with the ACV value at 1kHz. This simplifies the TVC correction, providing that a general rule is applied to account for the polarity sign.

General Rule:
When a 'plus' sign indicates that a larger value of ACV input than DCV input is required to produce the same output from a TVC, then the TVC flatness correction at Fc relative to 1kHz is given by:

(Fc correction figure) minus (1kHz correction figure)

This figure is **added** to the original 1kHz figure adjusted on the 4920M, to produce the value to be entered in 'SET' mode at Fc.

Example:
Say the original 1kHz output from the ACV source was adjusted to give a 4920M reading of 10.000,00V.

For a TVC whose 1kHz and 200kHz correction figures at 10V are -6ppm and -10ppm repectively, the flatness correction figure would be:

(-10ppm) - (-6ppm) = -4ppm.

The value entered in 'SET' mode at Fc should be:
10.000,00V + (-4ppm x 10.000,00V)
*= 10.000,00V + (-0.000,04V) = **9.999,96V***

To Calibrate:
Carry out the following procedure for the ACV ranges and the WBV 1V range, at the voltages and frequencies detailed in Table 1.4.1.

1. Configure a Thermal Voltage Converter for **Vc**.
2. Connect the AC Voltage Source into the calibration setup as shown in Figure 1.4.1.
3. On the 4920M, select the required function and range.
4. Set the output of the AC Source to **Vc** at **1kHz** and turn its output on.
5. Increment or decrement the output voltage of the AC Source until the 4920M reads as close as possible to **Vc**.
   Note the 4920M reading.
6. Allow the Thermal Voltage Converter to settle.
7. Adjust the DC Nanovolt Source to achieve a null on the DC Nanovoltmeter.
8. Set the AC Source to **Vc** at **Fc** (or within the frequency limits) then turn its output on.
9. Increment or decrement the output voltage of the AC Source to achieve a null on the DC Nanovoltmeter. Allow the Thermal Voltage Converter to settle. Then, if necessary, readjust the output voltage of the AC Source for null.
10. From the **SPCL** menu, select **Flat**, followed by **Set**.

(Refer to Note 2)

11. Calculate the voltage difference correction for the Thermal Voltage Converter at **Fc** relative to **1kHz**, at **Vc**. Use this figure to correct the 4920M reading noted in operation (**5**). In the **SET** menu, enter this corrected value, and press the **Enter** key.
12. Press the **Caltrig** key to execute the flatness calibration.

1.4.4.10 WBV 3V Range - Flatness Calibration setup

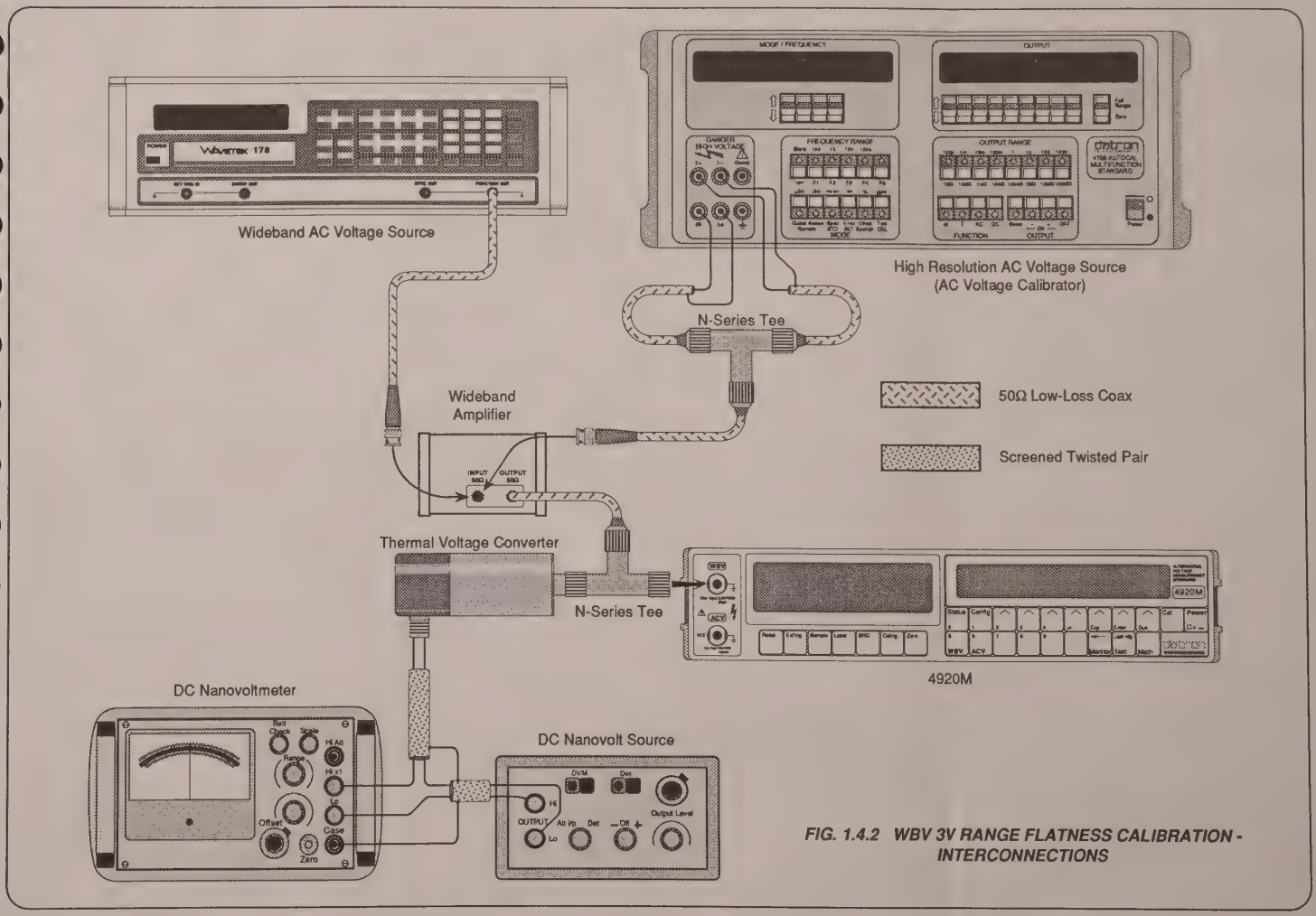


FIG. 1.4.2 WBV 3V RANGE FLATNESS CALIBRATION - INTERCONNECTIONS

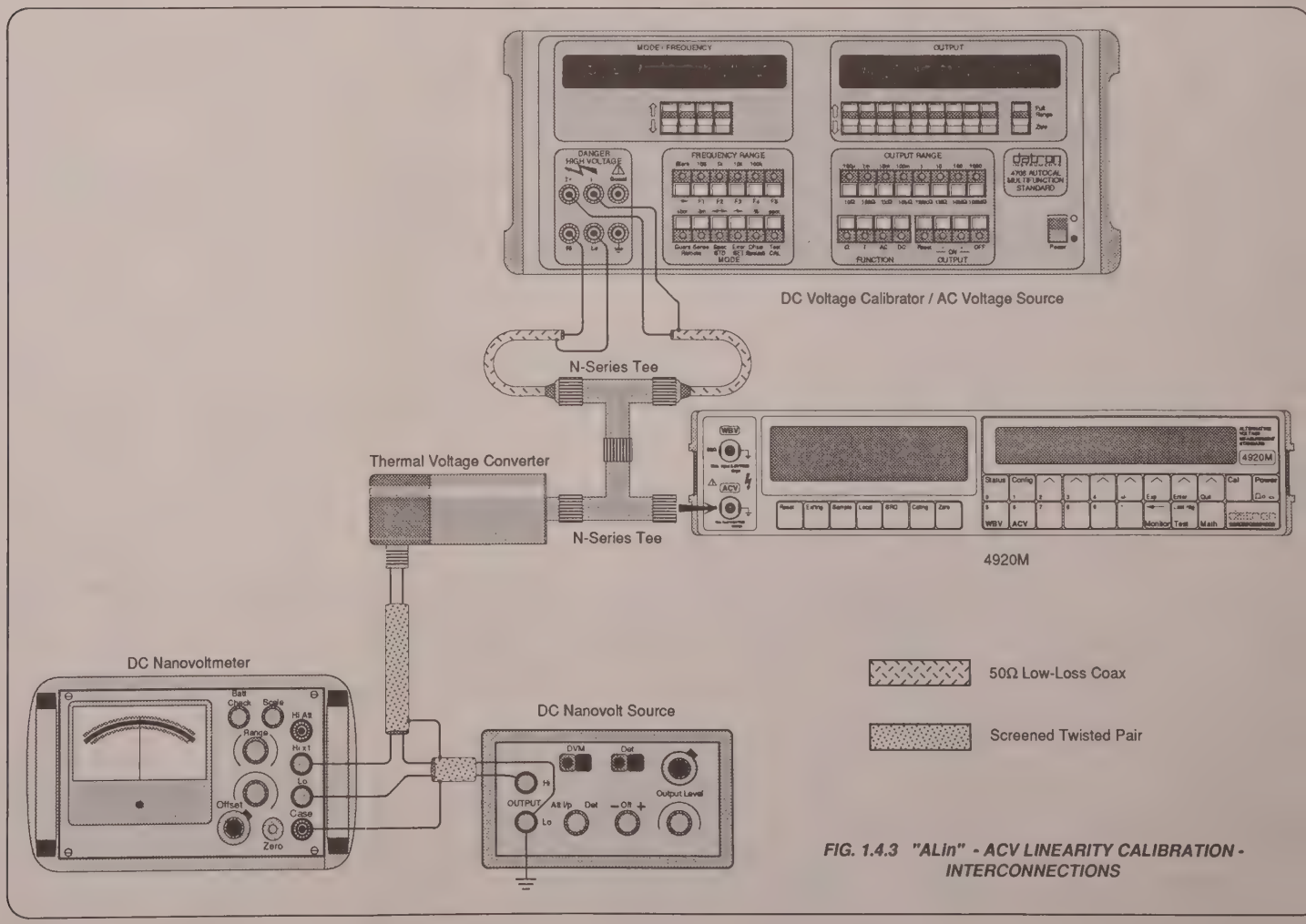


FIG. 1.4.3 "ALin" - ACV LINEARITY CALIBRATION - INTERCONNECTIONS

	Range	Calibration Voltage (Vc)	Recommended Frequency (Fc)	Lower Fc Limit	Upper Fc Limit
ACV	0.3V	300.0000mV	50kHz	9.8kHz	51kHz
	0.3V	300.0000mV	200kHz	98kHz	408kHz
	0.3V	300.0000mV	500kHz	490kHz	765kHz
	0.3V	300.0000mV	1MHz	882kHz	1.02MHz
ACV	1V	1.000000V	50kHz	9.8kHz	51kHz
	1V	1.000000V	200kHz	98kHz	408kHz
	1V	1.000000V	500kHz	490kHz	765kHz
	1V	1.000000V	1MHz	882kHz	1.02MHz
ACV	3V	3.000000V	50kHz	9.8kHz	51kHz
	3V	3.000000V	200kHz	98kHz	408kHz
	3V	3.000000V	500kHz	490kHz	765kHz
	3V	3.000000V	1MHz	882kHz	1.02MHz
ACV	10V	10.00000V	50kHz	9.8kHz	51kHz
	10V	10.00000V	200kHz	98kHz	408kHz
	10V	10.00000V	500kHz	490kHz	765kHz
	10V	10.00000V	1MHz	882kHz	1.02MHz
ACV	30V	30.00000V	50kHz	9.8kHz	51kHz
	30V	30.00000V	200kHz	98kHz	408kHz
	30V	30.00000V	500kHz	490kHz	765kHz
†	30V	19.99999V	1MHz	882kHz	1.02MHz
ACV	100V	100.0000V	50kHz	9.8kHz	51kHz
	100V	100.0000V	200kHz	98kHz	408kHz
†	100V	19.99999V	500kHz	490kHz	765kHz
†	100V	19.99999V	1MHz	882kHz	1.02MHz
ACV	300V	300.0000V	10kHz	4.9kHz	15.3kHz
	300V	300.0000V	30kHz	20.4kHz	40.8kHz
	300V	300.0000V	50kHz	49kHz	76.5kHz
	300V	300.0000V	100kHz	88.2kHz	102kHz
ACV	1kV	1000.000V	10kHz	4.9kHz	15.3kHz
	1kV	1000.000V	30kHz	20.4kHz	40.8kHz
	1kV	~~1000~~ 700.000V	50kHz	49kHz	76.5kHz
	1kV	~~1000~~ 700.000V	100kHz	88.2kHz	102kHz
WBV	1V	1.000000V	50kHz	9.8kHz	51kHz
	1V	1.000000V	200kHz	98kHz	408kHz
	1V	1.000000V	500kHz	490kHz	765kHz
	1V	1.000000V	1MHz	882kHz	1.02MHz

TABLE 1.4.1 ACV RANGES and WBV 1V RANGE FLATNESS: CALIBRATION POINTS

† *4920M can calibrate at a Vc of nominal full range value, if the calibrator can drive such an output.*

Calibrator can't do > 700 V @ 100 kHz

1.4.4.9 WBV 3V Range Flatness Calibration Procedure

Note 1
For flatness calibration of any currently selected range:
Vc is the required calibration voltage;
20MHz is the recommended frequency.

Note 2. TVC Calibration
In the following procedures, the Thermal Voltage Converter is used to allow the 1kHz signal level to be remembered by the setting of the DC Nanovolt Source which nulls the TVC DC output. The flatness error for 20MHz (relative to 1kHz) is measured by applying 20MHz to the TVC and adjusting the ACV source output to give the same null.

For this process to be accurate, it is necessary to account for the flatness of the TVC at 20MHz relative to 1kHz. The flatness figures are usually available in tabular form on the most-recent calibration certificate for the TVC in use.

The most usual method of recording the TVC response, at its calibrated frequencies, is to give a correction figure which is the incremental difference between the AC and DC inputs which produce the same output.

The difference is usually expressed in ppm with a polarity sign. On most calibration certificates, a 'plus' sign indicates that a higher value of ACV input is necessary to produce the same output as a DCV input.

In the procedure we do not compare ACV with DCV. For flatness calibration we need to compare the ACV value at 20MHz with the ACV value at 1kHz. This simplifies the TVC correction, providing that a general rule is applied to account for the polarity sign.

General Rule:
When a 'plus' sign indicates that a larger value of ACV input than DCV input is required to produce the same output from a TVC, then the TVC flatness correction at 20MHz relative to 1kHz is given by:

(20MHz correction figure) minus (1kHz correction figure)

This figure is **added** to the original 1kHz figure adjusted on the 4920M, to produce the value to be entered in 'SET' mode at 20MHz.

Example:
Say the original 1kHz output from the ACV source was adjusted to give a 4920M reading of 3.000,000V.

For a TVC whose 1kHz and 20MHz correction figures at 3V are -5ppm and -17ppm repectively, the flatness correction figure would be:

(-17ppm) - (-5ppm) = -12ppm.

The value entered in 'SET' mode at Fc should be:
3.000,000V + (-12ppm x 3.000,000V)
*= 3.000,000V + (-0.000,060V) = **2.999,964V***

To Calibrate:
Carry out the following procedure for the 3V WBV range, referring to Fig 1.4.2.

1. Configure the Thermal Voltage Converter for 3V.
2. Connect the High Resolution AC Voltage Source (AC Calibrator), Wideband Amplifer and Thermal Voltage Converter to the 4920M as shown in Figure 1.4.2.
3. Select **WBV** on the 4920M.
4. Set the High Resolution Source to 3V at 1kHz with output on. Turn the output of the Wideband Amplifier on.
5. Increment or decrement the output voltage of the High Resolution Source until the 4920M reads as close as possible to 3.000000V.
   Note the 4920M reading.
6. Allow the Thermal Voltage Converter to settle.
7. Adjust the DC Nanovolt Source to achieve a null on the DC Nanovoltmeter.
8. Turn the output of the High Resolution Source off and disconnect it from the input to the Wideband Amplifier.
9. Connect the Wideband AC Voltage Source to the input of the Wideband Amplifier as shown in Figure 1.4.2.
10. Set the output of the Wideband Source to 3V at 20MHz, and turn its output on.
11. Increment or decrement the output voltage of the Wideband Source to achieve a null on the DC Nanovoltmeter. Allow the Thermal Voltage Converter to settle. Then, if necessary, readjust the output voltage of the Wideband Source for null.
12. From the **SPCL** menu, select **Flat**, followed by **Set**.

(Refer to Note 2)
13. Calculate the voltage difference correction for the Thermal Voltage Converter at **20MHz** relative to **1kHz**, at **Vc**. Use this figure to correct the 4920M reading noted in operation (5).
    In the **SET** menu, enter this corrected value, and press the **Enter** key.
14. Press the **Caltrig** key to execute the flatness calibration.

1.4.5 ACV Linearity Calibration - 'ALin' Key

To calibrate all ACV ranges' linearities using a calibration in either the 10V range.

Note that the procedure is written for recommended voltages and frequencies.
The alternative voltages and frequencies are shown in Table 1.4.2, below.

Linearity Calibration at the Upper Calibration Point

1. Connect the DC Voltage Calibrator into the calibration setup as shown in Figure 1.4.3.
2. On the 4920M, select **ACV** function and the **10V** range. Press the **Cal** key and select **Spcl**. From the **SPCL** menu, select the **ALin** option.
3. Configure a Thermal Voltage Converter for 10V.
4. Set the output of the DC Calibrator to 10V, and turn its output on.
5. Allow the Thermal Voltage Converter to settle.
6. Adjust the DC Nanovolt Source to achieve a null on the DC Nanovoltmeter.
7. Reverse the polarity of the DC Calibrator output. Allow the Thermal Voltage Converter to settle, and note the DC reversal error on the DC Nanovoltmeter. Adjust the Nanovolt Source until the Nanovoltmeter shows half of the DC reversal error.
8. Turn the output of the DC Calibrator off and disconnect it by splitting the two precision N-series tees.
9. Connect the AC Voltage Source in place of the DC Voltage Calibrator. (Note: if the DC Calibrator and AC Voltage Source are combined into a single unit, the output of this unit can simply be switched from DC to AC.)
10. Set the AC Source to 10V RMS at 1MHz, and turn its output on.
11. Increment or decrement the output voltage of the AC Source to achieve a null on the DC Nanovoltmeter. Allow the Thermal Voltage Converter to settle. Then, if necessary, readjust the output voltage of the AC Source for null.
12. Select the **SET** option and enter a value which is equal to the calibration voltage used in operation (**4**), incremented or decremented by the AC-DC difference correction of the Thermal Voltage Converter at the calibration voltage and frequency.
13. Execute ALin calibration at the Upper calibration point by pressing the 4920M **Caltrig** key.

Linearity Calibration at the Lower Calibration Point

14. Repeat operations (**3**) to (**13**) for 2.0V at 1MHz.

ACV Linearity Calibration

Table 1.4.2 Upper and Lower Calibration Points - Permissible Voltages and Frequencies

Range	Upper Cal Point: Uc		Lower Cal Point: Lc	
	Recommended	Voltage Limits	Recommended	Voltage Limits
10V	10.0V	5.0V ≤ **Uc** <12V	2.0V	0.3V ≤ **Lc** < 5V

All Calibration Points - Permissible Frequency Fc:

Recommended: 1MHz **Limits:** 980kHz ≤ **Fc** ≤ 1.02MHz

1.4.6 Clear the Non-Volatile RAM Calibration Memory - 'ClrNV' Key

To clear all or part of the calibration memory

Caution!

This command can **obliterate** the results of an **expensive** original calibration or recalibration!

Extent of Clear

The extent of clear is defined by programming the following options:

All clears all non-volatile calibration memory *except* user-entered data.
The calibration interval is reset to 180 days,
The internal calendar/clock is reset to 121281.

ALin Clears the section of non-volatile calibration memory which contains corrections to ACV linearity.

Flat Clears the section of non-volatile calibration memory which contains corrections to flatness.

Gain Clears the section of non-volatile calibration memory which contains corrections to range gain.

ROM Checksums

ROM checksums are recalculated and written to calibration memory when any Clear NV RAM command is executed.

Special Calibration following Memory Corruption

(e.g. When the battery which supplies the non-volatile calibration memory has been changed with the power off - see Section 4)

Section 2 (Fault Diagnosis) describes the device-dependent error codes resulting from internal tests. Error codes which are generated for calibration memory faults are listed in Section 2.

Some of these refer to individual calibration correction errors, and others to combined errors.

When faced with any of these error codes, please seek advice or assistance from your nearest Datron Service Center.

When it is deemed necessary to carry out special calibration as a result of non-volatile memory corruption, the starting point should be to clear the relevant calibration memory before proceeding with other individual calibrations.

Clearance Procedure

Selecting **Clr NV** in the **SPCL** menu transfers to the **CLEAR NV RAM** menu which offers a choice of clearing one or all of four sections of RAM. The selection should be chosen as a result of consultation with technical staff at the service center.

When the selection is made by pressing the relevant soft menu key, the processor calculates and writes new bitsums. No NV RAM is cleared during this operation; the dot-matrix display merely shows the words **WRITING NEW BITSUMS**.

When the **CLEAR NV RAM** menu is restored, the selected (underlined) Calstore NV RAM can be irrevocably cleared by pressing the **Caltrig** key.

SECTION 2 GUIDE TO 4920M FAULT DIAGNOSIS

2.1 Introduction

2.1.1 Use of Error Codes

The 4920M incorporates an extensive set of error messages, each of which includes a 4-digit code number and descriptive text. These messages can summarize incorrect application programming via the IEEE 488 bus or keyboard, or a fault within the instrument.

2.1.2 Code Groupings

Consistency with IEEE 488.2

The instrument is programmed in firmware to monitor its own operation, including interface protocols used via the IEEE 488 bus. As a result it will generate certain error codes to indicate that routine operations (including remote operation and some aspects of external calibration) are unsuccessful. Other error codes can be generated only from internal tests which are part of particular facilities initiated by the user, such as Selftest.

Because the remote operation of the instrument is designed to conform to the IEEE 488.2 standard, the large-scale categories of errors decreed by the standard have been used as the general basis for all error-reporting. This means that error codes and messages reported on the front panel display are consistent, as far as possible, with those reported via the IEEE 488 bus.

The type-names given to groupings of errors are thus primarily determined by those described in the IEEE 488.2 Standard specifications. Some categories apply only to bus operation, and are covered in Section 5 of the User's Handbook. Those which can be useful for diagnosing faults within the instrument are described in this section.

Non-Recoverable Errors

For all **Fatal System Errors**, the error condition is reported by a message on the front panel right-hand display. The processor halts after displaying the message. The unit must be power-cycled to regain control.

Recoverable Errors

These consist of **Command Errors, Execution Errors** and **Device-Dependent Errors.**

Command Error

This can occur only when under remote control. No error message is generated. A Command Error results from use of illegal syntax or illegal sequencing of 488.2 commands, and is cleared by re-programming. It is reported via the Status Reporting mechanism described in Section 5 of the User's Handbook.

Execution Error

This can occur in either Local or Remote operation. An Execution Error indicates that a command cannot be executed (e.g. CAL SWITCH DISABLED). It is reported over the IEEE 488 bus using the Status Reporting mechanism described in Section 5 of the User's Handbook and an error message is presented on the front panel right-hand display. The error can be cleared by reprogramming, but the message remains available in the remote error queue until it is read destructively.

Device-Dependent Error

This can occur in either Local or Remote operation. A Device-Dependent Error indicates that execution of a user command has failed to reach a successful completion. It is reported over the IEEE 488 bus using the Status Reporting mechanism described in Section 5 of the User's Handbook and an error message is presented on the front panel right-hand display. The error can be cleared by reprogramming, but the message remains available in the remote error queue until it is read destructively.

2.1 Introduction (Contd.)

2.1.3 'Operational' and 'Diagnostic' Selftest

The front-panel test facilities are summarized in Section 4 of the User's Handbook (*page 4-16*). Two forms of self-test are available in the TEST menu, obtained by pressing the Test hard key:

Diagnostic Selftest
This checks:

Digital Assembly:	Power; Memory; Calibration Validity.
A-D Assembly:	Reference Voltage; A-D Operation.
ACV Assembly:	Ranges; Filters; Frequency Measurement.
WBV Assembly:	Ranges; Input Impedance.

Most tests consist of measuring a voltage and checking deviation against tolerance. If deviation is less than 100% of tolerance it is presented on the left-hand display at the conclusion of the test step. When a failure is detected, the test halts and cannot be resumed.

Operational Selftest
This is a subset of the set of tests allocated to a Diagnostic Selftest. It is intended as a quick 'Confidence' check to show that no serious defect is present to affect the instrument's operation. To increase the speed, deviation % is not displayed. When a failure is detected, the test halts, but may be resumed.

2.1.4 References in this Section

The messages are interpreted in this section to assist in fault localization:

Fatal System Errors:	2.2
Command Errors:	2.3
1000 Series Codes - Execution Errors:	2.4
Device-Dependent Errors - Index:	2.5
4000 Series Codes - Fault Localization:	2.6
Test Descriptions:	2.7

2.2 9000 Series Codes - Fatal System Errors

2.2.1 Introduction

System errors which cannot be recovered cause the system to halt with a message displayed (the processor stops after displaying the message). The error condition is reported only via the front panel, but this may fail if the fault is severe enough and unfortunately located.

2.2.2 Immediate Action

1. Record any Error Code and accompanying message displayed on the front panel. Also record the hardware environment and any operations in progress at the time of failure. Fatal System errors are generally caused by hardware or software faults.
2. Power OFF and ON again to try to restart operation.
3. If (2) is unsuccessful, power OFF again and allow the instrument to cool for 15 minutes; then try powering ON.
4. If the error condition does not recur, repeat the original operations. Check that no temperature or configuration factors cause the error condition to return. If successful, carefully proceed with further measurements as required.
5. If (2) or (3) do not clear the error condition, or if it recurs in (4); further investigation of the fault will be required.

2.2.3 Fatal System Error Codes

Code	Type of Fault	
9000	System Kernel Fault:	Corruption of scheduling queue.
9001	Run Time System Error:	Illegal parameter value.
9002	Unexpected Exception:	Attempt to write to non-RAM etc.
9005	Serial Interface Fault:	Unrecoverable error in serial interface data transmission.
9099	Undefined Fatal Error	

2.3 Command Errors

2.3.1 Generation

A Command Error occurs when a received bus command does not satisfy the IEEE 488.2 generic syntax or the device command syntax programmed into the instrument interface's parser, and so is not recognized as a valid command. Command errors do not have an associated queue.

2.3.2 Local Operation

Command Errors cannot be generated in local operation.

2.3.3 Remote Operation

Command Errors are reported over the IEEE 488 bus, in remote operation. The CME bit (5) is set true in the Standard-defined Event Status Byte, but there is no associated queue so no index can be given.

The error is reported by the mechanisms described in Section 5 of the User's Handbook, in the sub-section dealing with status reporting.

2.4 1000 Series Codes - Execution Errors

2.4.1 Generation

An Execution Error indicates that a command has been recognised as valid (i.e. it can be parsed, and does not generate a Command Error), but cannot be executed because it is incompatible with the current device state, or because it attempts to command parameters which are out-of-limits.

2.4.2 Local Operation

Front panel operation is designed to lock out the conditions which would give rise to execution errors, by not offering the erroneous choices in the appropriate menus. However, some actions can be taken (such as entering numeric data which lies outside the range for the selected parameter) which cannot be locked out.

In these cases the Execution error is used as an aide-memoire for the user's convenience. The error code number appears on the front panel dot-matrix display, accompanied by an error message.

2.4.3 Remote Operation

The EXE bit (4) is set true in the Standard-defined Event Status Byte, and the error code number is appended to the Execution Error queue. The error is reported by the mechanisms described in Section 5 of the User's Handbook, in the sub-section dealing with status reporting.

The queue entries can be read destructively as LIFO by the Common query command *EXQ?.

2.4.4 Execution Error Codes

Code	Type of Error
1000	No Execution Error
1001	No Test in Cal Mode
1002	Resume Test not allowed
1003	Cal Switch disabled
1004	Cal Mode not enabled
1005	Set Nominal not allowed
1006	Invalid Range/Function
1007	Invalid Numeric Data

2.5 Device-Dependent Errors - Index

2.5.1 Introduction

A Device-Dependent Error (DDE) is generated if the device detects an internal operating fault (eg. during self-test), or if certain user-operations are invalid.

Note that error codes beginning 2... can be caused by incorrect operation or instrument failure; error codes beginning 3... are almost certainly due to instrument failure. Error codes 4... are the result of Selftest failure.

When a DDE occurs, the operation in progress is aborted.

2.5.2 Local Operation

The code number and description appear on the right-hand display, remaining visible until the next key-press or remote command and placed at the head of the error queue.

2.5.3 Remote Operation

In Remote, the error is reported by the mechanisms described in Section 5 of the User's Handbook, in the sub-section dealing with status reporting. The queue entries can be read destructively as LIFO by the query DDQ?.

2.5.4 Index of Device-Dependent Error Codes - Normal and Calibration Operations

Normal Operation

2000 No Device Error in List
2006 Invalid Calstore Read

2009 Invalid Serial Data
2010 Corrupt Datarec Value

Calibration Invalidities

2001 Invalid Gain Cal
2002 Invalid HF Trim Cal
2003 Invalid Flatness Cal
2004 Invalid Linearity Cal
2005 Invalid Frequency Cal
2007 Invalid Calstore Write
2008 Invalid Cal Arithmet

Serial Loop Initialization

3028 Chip Test AC Pre-amp
3029 Chip Test AC RMS Control
3030 Chip Test A-to-D DAC
3031 Chip Test A-to-D Switch
3032 Chip Test A-to-D Tester

3033 Serial Loop Failure

Calibration Illegalities

3001 Illegal Cal Exercise
3002 Illegal Special Cal Step
3003 Illegal Cal Update
3004 Illegal Calstore Access
3005 Illegal Calstore Clear
3006 Illegal Calstore Func
3007 Illegal Calstore Range
3008 Illegal Calstore Length
3009 Illegal Clock Destinatn
3010 Illegal Clock Reading
3011 Illegal Clock Setting
3012 Illegal Clock Access
3013 Illegal Measure Phase
3014 Illegal Scale Index
3015 Illegal Flatness Value
3016 Illegal Linearity Value
3017 Illegal HF Correction
3018 Illegal Gain Correction
3019 Illegal WBLIN Parameter
3020 Illegal WB RMS Value
3021 Illegal WB DAC Setting
3022 Illegal WB Autorange Func
3023 Illegal WB Autorange Range
3024 Illegal WB Test Stage
3025 Illegal WB Test Store
3026 Illegal WB Test Polarity
3027 Illegal Enginr Op-Code
3034 Illegal Operation
3035 Illegal Parameter

2.5.5 Index of Device-Dependent Error Codes - Selftest Operations

Note that errors from 4015 to 4052 may occur if a signal or low impedance is connected to either instrument input when the test is taking place. If this is not the case, then a self-test error implies instrument failure.

Code	Description	Most Probable Cause
Preliminary		
4000	Stuck Key.	**Keyboard**
4001	Dig Power Supplies	**Digital PCB Assembly**
4002	Battery Voltage	
Memory		
4003	ROM Bitsums.	
4004	RAM Read/Write.	
4005	CAL Integrity.	
Digital Communication		
4006	Serial Loop Config.	**Digital, A-D or ACV PCB Assembly**
Analog-to-Digital Conversion		
4007	A-to-D Zero.	**A-D PCB Assembly**
4008	A-to-D +15V Supply.	
4009	A-to-D -15V Supply.	
4010	A-to-D Gain.	
4011	A-to-D Linearity +.	
4012	A-to-D Linearity -.	
4013	A-to-D +11V Supply.	
4014	A-to-D -19V Supply.	
High Accuracy ACV Conditioning		
4015	AC Preamp X1 Zero.	**ACV Preamp Assembly**
4016	AC Preamp X3 Zero.	
4017	AC 1V Gain, DC Pos.	
4018	AC 1V Gain, DC Neg.	
4019	AC Preamp X3 Gain.	
4020	AC 10V Attenuator.	
4021	AC 100V Attenuator.	
4022	AC 1kV Attenuator.	
Frequency and Overload		
4023	AC Freq Counter.	**ACV Main Assembly**
4024	AC Overload Detect.	
4025	AC Overload Switch.	

Code	Description	Most Probable Cause
High Accuracy RMS Conversion		
4026	AC HF Path Detect.	
4027	AC RMS Converter.	
4028	AC RMS Track.	
4029	AC RMS Hold.	
4030	AC Quasi-Sine.	**ACV Main PCB Assembly**
4031	AC Measurement.	
4032	Not Used.	
4033	AC 10Hz Filter.	
4034	Not Used.	
4035	AC RMS Linearity.	
Wide Band D-A Conversion		
4036	WB DAC +ve Zero.	
4037	WB DAC -ve Zero.	
4038	WB DAC +ve Full Scl.	**A-D PCB Assembly**
4039	WB DAC -ve Full Scl.	
4040	WB DAC +3.5V.	
4041	WB DAC -3.5V.	
Wide Band Chopper Action		
4042	WB DC Switch +ve.	
4043	WB DC Switch -ve.	
Wide Band Thermal Conversion		
4044	WB TTU DC 3.5V.	
4045	WB TTU DC 1.0V.	
4046	WB TTU DC 0V.	
4047	WB TTU AC 0V.	**WBV PCB Assembly**
4048	Not Used.	
Wide Band Measurement Paths		
4049	A-to-D WB Path.	
4050	WB Input Path.	
4051	WB Input Z, DC Chan.	
4052	WB 100mV Path.	
4053	WB Cal Validity.	
Other		
4054	Bus Address.	

2.6 4000 Series Codes - Fault Localization

2.6.1 Selftests

(Refer to User's Handbook; Section 4, page 4-16)

The 4920M firmware incorporates a program to run a comprehensive selftest of the instrument's operating parameters, utilizing an internal reference as a source to stimulate measurements for the test.

There are two versions of the test: 'Operational', and 'Diagnostic'. Both tests activate the same series of over 50 checks of operating parameters, in the same order. The main difference between the two is that the diagnostic test also presents quantitative measurement results to the operator as the test proceeds.

Failure to meet the accuracy tolerance for any one of the parameters will generate an error code.

2.6.1.1 'OPER': Operational Selftest

This selftest runs automatically at power on.

Operational selftest is accessed by pressing the front panel **Test** key then selecting **Oper** in the **TEST** menu. This opens the **OPER TEST** menu and starts the test sequence, which runs for some 3 minutes if no errors are found. As the sequence proceeds, the dot-matrix display is updated with the name of the current test.

If any test has results which are out of test limits, then the sequence stops and the **OPER FAIL** menu is presented. A 4000-series error code is given, followed by a brief test description (the format can be seen by powering the intrument on while pressing one of the front panel keys).

The test can be continued by pressing **Cont** in the **OPER FAIL** menu. The **OPER TEST** menu is reinstated, and updated as before. When the sequence is finished, the word **COMPLETED** appears on the **OPER TEST** menu.

2.6.1.2 'DIAG': Diagnostic Selftest

Diagnostic selftest is accessed by pressing the front panel **Test** key then selecting **Diag** in the **TEST** menu. This opens the **DIAG TEST** menu and starts the test sequence, which runs for some 5 minutes if no errors are found. As the sequence proceeds, the dot-matrix display is updated with the name of the current test.

Once a diagnostic test measurement has been completed, and before the sequence moves on to the next test, a percentage value appears for a short time on the main display. This represents the accuracy of the result of the measurement, as a percentage of the total tolerance permitted for that parameter. Otherwise, the sequence of tests, and the test tolerances, are the same as for the Operational selftest.

When the sequence is finished, the word **COMPLETED** appears on the **DIAG TEST** menu.

If any test has results which are out of test limits, then the sequence stops and the **DIAG FAIL** menu is presented. A 4000-series error code is given, followed by a brief test description. Once this stage has been reached, the test cannot be continued.

2.7 Test Descriptions

2.7.1 General

The purpose of this sub-section is to show how to activate individual tests from the Diagnostic Selftest sequence, describe the nature of each test and identify the part of the instrument which is being checked. References to Volume 2 of this handbook identify test paths on the circuit diagrams in Section 11.

The descriptions are indexed by error code. Each description gives the test path number; test type; input path; measurement path; and the tolerance limits allocated to each measurement.

2.7.2 Selftest Error Codes

The codes for the Selftest operations are the individual test numbers in the sequence of checks or calibrations implemented by the processor. They will appear as Error Codes only if the process has not been successful, providing data for fault diagnosis. If the fault cannot be diagnosed locally, the data should be recorded and reported for interpretation to your nearest Datron Service Center.

2.7.3 Test Pathways

A 'Path' number (prefixed by a capital 'P') describes a single test arrangement, in which sufficient readings are taken to establish a statistical field of results. Significant measurements are made by processing the results through appropriate digital calculations. Results are compared against specific limits of tolerance allocated in that particular setup for the tested parameter.

2.7.4 Access to Test Pathways via the 4920M Menu Keys

2.7.4.1 Reading the Error Codes

Each of the two forms of self test runs at high speed, and does not stop unless an error is discovered. When the test does stop, the error code for the failure is shown on the Menu display. Once an error code appears on the display, it should be noted.

Each error code is associated with a unique test pathway, whose path number is shown in the test description (indexed by error code).

2.7.4.2 Access to Pathway Information

Certain menu keys allow a user to select test paths. When a path number is selected, live measurements are carried out for the path (the same as during the selftest), and the results are presented on the Main Display. These can be compared against the limits shown in the test description which carries the same path number.

The path measurement reading on the Main Display is normalized to the range which was already selected. So before using the pathway keys it is advisable to select the 10V ACV range, to obtain readings which are approximately volts (uncalibrated reading).

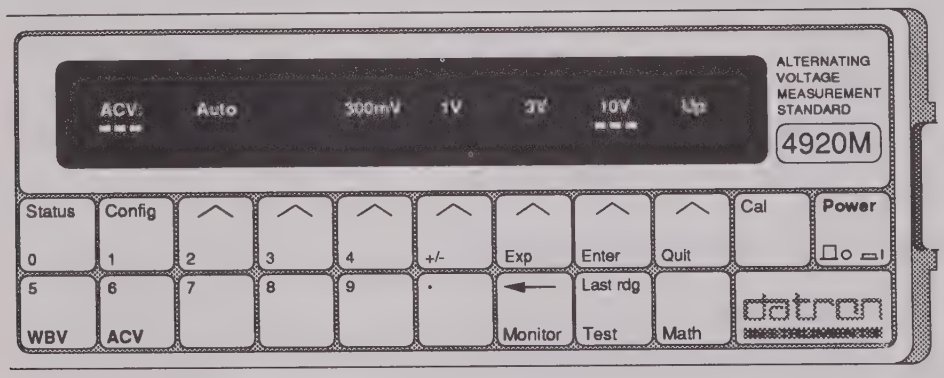
2.7.5 Activating the Test Pathway

The method of activating the paths using path numbers is illustrated in the following diagrams.

Start by looking in the Test List (Sect 2.7.6) for the test description indexed by the error code which appeared when the Selftest stopped. Read off the associated pathway number.

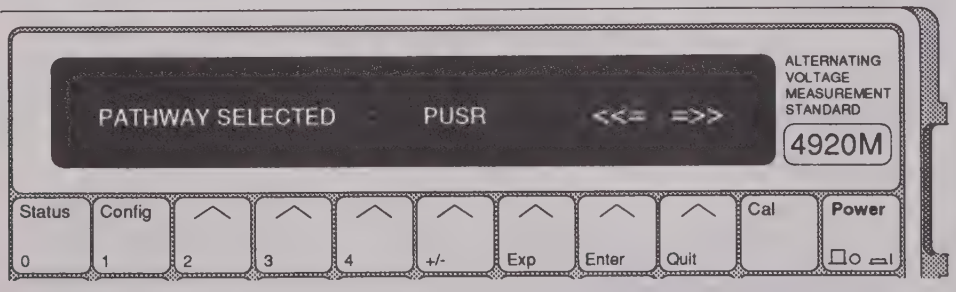
Select the 1V ACV Range

☞ Press the ACV key and then the '10V' soft key:



Select the Pathway Facility

☞ Press the Status key, then the Config key; and finally the soft key labelled '+/-'



PUSR indicates that the present pathway is as defined by the user's previous selection of front panel keys;

<<= *(Enter)* decrements the path number by 1;

=>> *(Quit)* increments the path number by 1.

Press the ==>> soft key seven times. For each press, four characters appear in place of PUSR. Ignore these characters; they are not measurement pathways. Press ==>> once again. This selects pathway PV01; the next press selects pathway PV02, and so on up to PV08 (A-D tests).

By pressing ==>> again, pathway PA01 is activated; the next press selects pathway PA02, and so on up to PA22 (High Accuracy ACV tests).

Further use of the ==>> key activates the WBV test pathways, from PW01 to PW17. After PW17, and a further selection P001, the selection reaches PUSR again.

Use of the <<== key runs through the pathways in the reverse order.

2.7.6 List of Diagnostic Tests

2.7.6.1 A-D Tests

4007 **PV01** **A-D Zero Check** (A-D pcb)
Pathway: Hard Zero via Ref MUX (U301-9) to INT_SIG_BUS and A-D MUX (U401-6).
Measure: via A-D.
Test Limits | A-D zero | ≤ 10mV

4008 **PV02** **+15V Check** (A-D pcb)
Pathway: +5V from +15V via R301 & Ref MUX (U301-11) to INT_SIG_BUS and A-D MUX (U401-6).
Measure: via A-D.
Test Limits +4.5V ≤ Rdg ≤ +5.5V

4009 **PV03** **-15V Check** (A-D pcb)
Pathway: -5V from -15V via R306 & Ref MUX (U301-12) to INT_SIG_BUS and A-D MUX (U401-6).
Measure: via A-D.
Test Limits -5.5V ≤ Rdg ≤ -4.5V

4010 **PV04** **REF 2 Check** (A-D pcb)
Set: INT_SIG_BUS to Zero (U301-9).
Pathway: Ref 2 (U402 O/P) to A-D MUX (U401-10).
Measure: via A-D.
Test Limits 6.45V ≤ REF 2 ≤ 7.45V

4011 **PV05** **VREF2_POS Check** (+Ref/16), (A-D pcb)
Set: INT_SIG_BUS to Zero (U301-9).
Pathway: VREF2_POS (U406-7 O/P) to A-D MUX (U401-12).
Measure: via A-D.
Test Limits 1.760V ≤ VREF2_POS ≤ 1.860V

4012 **PV06** **VREF2_NEG Check** (-Ref/16), (A-D pcb)
Set: INT_SIG_BUS to Zero (U301-9).
Pathway: VREF2_NEG (U406-1 O/P) to A-D MUX (U401-11).
Measure: via A-D.
Test Limits -1.860V ≤ VREF2_NEG ≤ -1.760V

4013 **PV07** **+11V Supply Check** (A-D pcb)
Set: INT_SIG_BUS to Zero (U301-9).
Pathway: +7.28V from +11V (via R402/403) to A-D MUX (U401-9).
Measure: via A-D.
Test Limits +6.550V ≤ Rdg ≤ +8.010V

4014 **PV08** **-19V Supply Check** (A-D pcb)
Pathway: -6.6V from -19V via R309/R308 & Ref MUX (U301-11) to INT_SIG_BUS and A-D MUX (U401-6).
Measure: via A-D.
Test Limits -7.22V ≤ Rdg ≤ -6.12V

2.7.6.2 High Accuracy (ACV) Tests

4015 PA01 AC Preamp X1 Zero Check
Pathway: Hard Zero via Ref MUX (A-D pcb U301-9) and INT_SIG_BUS to preamp input (K1-6 on Hi Acc ACV pcb).
Range: ACV 1V range selected.
Measure: Preamp output AC_SENSE_SIG (Q104 on Hi Acc ACV pcb) via A-D MUX (A-D pcb U401-7).
Test Limits | X1 Zero | ≤ 1mV

4016 PA02 AC Preamp X3 Zero Check
Also Checks that loop is closed on X3 range.
Pathway: Hard Zero via Ref MUX (A-D pcb U301-9) and INT_SIG_BUS to preamp input (K1-6 on Hi Acc ACV pcb).
Range: ACV 0.3V range selected.
Measure: Preamp output AC_SENSE_SIG (Q104 on Hi Acc ACV pcb) via A-D MUX (A-D pcb U401-7).
Test Limits | X3 Zero | ≤ 3mV

4017 PA03 AC Preamp 1V Range - Gain Check for Positive Signals
Pathway: +1V via Ref MUX (A-D pcb U301-6) and INT_SIG_BUS to preamp input (K1-6 on Hi Acc ACV pcb).
Range: ACV 1V range selected.
Measure: Preamp output AC_SENSE_SIG (Q104 on Hi Acc ACV pcb) via A-D MUX (A-D pcb U401-7).
Test Limits +0.850V ≤ Rdg ≤ +1.050V

4018 PA04 AC Preamp 1V Range - Gain Check for Negative Signals
Pathway: -1V via Ref MUX (A-D pcb U301-7) and INT_SIG_BUS to preamp input (K1-6 on Hi Acc ACV pcb).
Range: ACV 1V range selected.
Measure: Preamp output AC_SENSE_SIG (Q104 on Hi Acc ACV pcb) via A-D MUX (A-D pcb U401-7).
Test Limits -1.050V ≤ Rdg ≤ -0.850

4019 PA05 AC Preamp - X3 Gain Check
Pathway: +1V via Ref MUX (A-D pcb U301-6) and INT_SIG_BUS to preamp input (K1-6 on Hi Acc ACV pcb).
Range: ACV 0.3V range selected.
Measure: Preamp output AC_SENSE_SIG (Q104 on Hi Acc ACV pcb) via A-D MUX (A-D pcb U401-7).
Test Limits +2.550V ≤ Rdg ≤ +3.150V

4020 PA06 AC Preamp - 10V Attenuator Check
Pathway: -7V via Ref MUX (A-D pcb U301-11) and INT_SIG_BUS to preamp input (K1-6 on Hi Acc ACV pcb).
Range: ACV 10V X3 selected.
Measure: Preamp output AC_SENSE_SIG (Q104 on Hi Acc ACV pcb) via A-D MUX (A-D pcb U401-7).
Test Limits -1.950V ≤ Rdg ≤ -1.550V

4021 PA07 AC Preamp - 100V Attenuator Check
Pathway: -7V via Ref MUX (A-D pcb U301-11) and INT_SIG_BUS to preamp input (K1-6 on Hi Acc ACV pcb).
Range: ACV 100V X3 selected.
Measure: Preamp output AC_SENSE_SIG (Q104 on Hi Acc ACV pcb) via A-D MUX (A-D pcb U401-7).
Test Limits -0.195V ≤ Rdg ≤ -0.155V

4022 PA08 AC Preamp - 1000V Attenuator Check
Pathway: -7V via Ref MUX (A-D pcb U301-11) and INT_SIG_BUS to preamp input (K1-6 on Hi Acc ACV pcb).
Range: ACV 1000V X3 selected.
Measure: Preamp output AC_SENSE_SIG (Q104 on Hi Acc ACV pcb) via A-D MUX (A-D pcb U401-7).
Test Limits -0.032V ≤ Rdg ≤ -0.020V

2.7.6.2 High Accuracy (ACV) Tests (Contd)

4023 PA09 AC Preamp - AC Frequency Counter Check

Pathway: 'CHOP' from U509-39 (DIVN) via Ref MUX (A-D pcb U301-10) and INT_SIG_BUS to preamp input (K1-6 on Hi Acc ACV pcb).
Range: ACV 1V selected.
Measure: Frequency output via Freq. Det (Hi Acc ACV pcb Q101) and Freq Counter (Hi Acc ACV pcb U604).

Frequency Error | Ef | < 1000ppm

4024 PA10 AC Preamp - AC Overload Detector Check

Checks: that a 'test' overload level in the ACV Pre-amp is detected, forcing the output to overload.
Set: 'OL_TEST' from U507-7 (Hi Acc ACV pcb) via (Hi Acc ACV pcb Q105), OL_LEV (Hi Acc ACV pcb Q605), OL_L (Hi Acc ACV pcb Q504-3, Q505-7/8), OL_FORCE (Hi Acc ACV pcb U204 gain via D201)
Range: ACV 1V selected.
Measure: HIACC_AC output direct via A-D MUX (A-D pcb U401-5). (A and C at logic-1; B at logic-Ø.)

Test Limits HIACC_AC > +6V

4025 PA12 AC Preamp - AC Overload Operation Check

Checks: that a detected overload automatically introduces the 1000V attenuator.
Pathway: -7V (A-D pcb U301-11) via INT_SIG_BUS to Hi Acc ACV pcb (relay K1-6).
Set: 'OL_TEST' from U507-7 (Hi Acc ACV pcb) via (Hi Acc ACV pcb Q105), OL_LEV (Hi Acc ACV pcb Q605), OL_L (Hi Acc ACV pcb Q504-3, Q505-7/8), OL_FORCE (Hi Acc ACV pcb U204 gain via D201)
Range: ACV 1V X 3 selected.
Measure: Preamp output AC_SENSE_SIG (Q104 on Hi Acc ACV pcb) via A-D MUX (A-D pcb U401-7).

Test Limits | AC_SENSE_SIG | < 50mV

4026 PA13 WB 50Ω Input Matching - HF Path DC Check

Checks: WBV 50Ω termination direct.
Set: (WBAC pcb) '100mVHF-H' to logic-1 energizes relay K101.
(Hi Acc AC pcb) 'WBAC_DRV' to logic-1 energizes relay K101.
Pathway: +1V from +5V via R102 (A-D pcb K101-9) and 50Ω input of WBAC pcb.
Range: WBV 100mVHF selected (1V range).
Measure: WBV input voltage at 50Ω termination via E101 (WBAC pcb), Hi Acc AC pcb U101-5, AC_SENSE_SIG (Q104 on Hi Acc ACV pcb) and A-D MUX (A-D pcb U401-7).

Test Limits -1.9V ≤ AC_SENSE_SIG

4027 PA14 AC RMS Detector - Loop Check

Checks: RMS Converter path direct.
Set: Hi Acc ACV pcb: Transfer commands A and C at logic-1; B at logic-Ø.
Pathway: 'CHOP' from U509-39 (DIVN) via Ref MUX (A-D pcb U301-10) and INT_SIG_BUS to preamp input (K1-6 on Hi Acc ACV pcb).
Range: ACV 1V selected.
Measure: Preamp output AC_SENSE_SIG (Q104 on Hi Acc ACV pcb) via A-D MUX (A-D pcb U401-7). (A and C at logic-1; B at logic-Ø.)
Store: Measured reading as 'M1'.

Test Limits 2.400V ≤ M_1 ≤ 3.000V

4028 PA15 AC RMS Detector - Sample and Hold Track Check

Checks: Sample and Hold Track.
Set: Hi Acc ACV pcb: Transfer commands A and B at logic-1; C at logic-Ø.
Pathway: 'CHOP' from U509-39 (DIVN) via Ref MUX (A-D pcb U301-10) and INT_SIG_BUS to preamp input (K1-6 on Hi Acc ACV pcb).
Range: ACV 1V selected.
Measure: Preamp output AC_SENSE_SIG (Q104 on Hi Acc ACV pcb) via A-D MUX (A-D pcb U401-7). (A and C at logic-1; B at logic-Ø.)
Store: Measured reading as 'M2'.

Test Limits (M_1 - 10mV) ≤ M_2 ≤ (M_1 + 10mV)

4029 **PA16** **AC RMS Detector - 'Hold' Operation Check**
Set: Hi Acc ACV pcb: Transfer commands A and C at logic-Ø; B at logic-1.
Pathway: 'CHOP' from U509-39 (DIVN) via Ref MUX (A-D pcb U301-10) and INT_SIG_BUS to preamp input (K1-6 on Hi Acc ACV pcb).
Range: ACV 1V selected.
Measure: Preamp output AC_SENSE_SIG (Q104 on Hi Acc ACV pcb) via A-D MUX (A-D pcb U401-7). (A and C at logic-1; B at logic-Ø.)
Store: Measured reading as 'M3'.
Test Limits $(M2 - 10mV) \leq M3 \leq (M2 + 10mV)$

4030 **PA17** **AC RMS Detector - Quasi-Sinewave Check**
Checks: RMS value of quasi-sinewave.
Set: Hi Acc ACV pcb: Transfer commands A and B at logic-Ø; C at logic-1.
Pathway: Held M2 from Sample and Hold to Quasi-Sine Generator divider as V_O.
Measure: Quasi-Sinewave RMS value via RMS Converter and A-D.
Test Limits $(M2 - 150mV) \leq$ Q-S RMS value $\leq (M2 + 150mV)$

4031 **PA18** **AC RMS Conversion - Full Measurement Check (100Hz Filter)**
Checks: RMS value of input to Hi Acc ACV system, via 100Hz filter path.
Set: Hi Acc ACV pcb: Transfer commands to follow normal three-measurement sequence. 100Hz Filter.
Pathway: 'CHOP' from U509-39 (DIVN) via Ref MUX (A-D pcb U301-10) and INT_SIG_BUS to preamp input (K1-6 on Hi Acc ACV pcb).
Measure: RMS value of input via RMS Converter and A-D.
Store: Measured reading as 'F1'.
Test Limits $2.550V \leq$ RMS value of input $\leq 2.850V$

PA19 **Pathway not used in 4920M**

4033 **PA20** **AC RMS Conversion - Full Measurement Check (10Hz Filter)**
Checks: RMS value of input to Hi Acc ACV system, via 10Hz filter path.
Set: Hi Acc ACV pcb: Transfer commands to follow normal three-measurement sequence. 10Hz Filter.
Pathway: 'CHOP' from U509-39 (DIVN) via Ref MUX (A-D pcb U301-10) and INT_SIG_BUS to preamp input (K1-6 on Hi Acc ACV pcb).
Measure: RMS value of input via RMS Converter and A-D.
Test Limits $(F1 - 30mV) \leq$ RMS value of input $\leq (F1 + 30mV)$
[Where F1 is the stored value from the test for PA18.]

PA21 **Pathway not used in 4920M**

4035 **PA22** **AC RMS Conversion - Linearity Check (10V Range)**
Checks: RMS value of input to Hi Acc ACV system.
Set: Hi Acc ACV pcb: Transfer commands to follow normal three-measurement sequence. 100Hz Filter.
Range: ACV 10V selected.
Pathway: 1V AC 'CHOP' signal from U509-39 (DIVN) via Ref MUX (A-D pcb U301-10) and INT_SIG_BUS to preamp input (K1-6 on Hi Acc ACV pcb).
Measure: RMS value of input via RMS Converter and A-D.
Test Limits $2.350V \leq$ RMS value of input $\leq 2.450V$

2.7.6.3 Wide Band (WBV) Tests

4036 **PW01** **WB DAC +ve Zero Check**

Set: WBV DAC to 0V using Serial Bus. ACHF-L active by Serial Bus (TTU input connected to front panel socket). Enable DCFB+ by HFD0-H.
Range: WBV 3V selected.
Pathway: WBV DAC output 'OUT1' (A-D pcb U201-1) via J107-4 to WBV pcb J201-10 to U201-2. From U201-1 to U201-6; U201-7, via U203-3/2 enabled, to J201-2 'WB_AC'. A-D PCB J107-3 to U401-4 A-D MUX.
Measure: DC Level of WB_AC via A-D (DAC and buffer offsets)

Test Limits Offset ≤ ±2mV

4037 **PW02** **WB DAC -ve Zero Check**

Set: WBV DAC to 0V using Serial Bus. ACHF-L active by Serial Bus (TTU input connected to front panel socket). Enable DCFB- by HFD1-H.
Range: WBV 3V selected.
Pathway: WBV DAC output 'OUT1' (A-D pcb U201-1) via J107-4 to WBV pcb J201-10 to U201-2. From U201-1 via U203-6/7 enabled, to J201-2 'WB_AC'. A-D pcb J107-3 to U401-4 A-D MUX.
Measure: DC Level of WB_AC via A-D (DAC and inverter offsets)

Test Limits Offset ≤ ±2mV

4038 **PW03** **WB DAC +ve Full Scale Check**

Set: WBV DAC to Full Scale (3.66V) using Serial Bus. ACHF-L active by Serial Bus (TTU input connected to front panel socket). Enable DCFB+ by HFD0-H.
Pathway: WBV DAC output 'OUT1' (A-D pcb U201-1) via J107-4 to WBV pcb J201-10 to U201-2. From U201-1 to U201-6; U201-7, via U203-3/2 enabled, to J201-2 'WB_AC'. A-D PCB J107-3 to U401-4 A-D MUX.
Measure: DC Level of WB_AC via A-D (checks performance of DAC Reference, DAC and DAC buffer at full scale).
Store: Measured reading as 'V1'

Test Limits 3.47V ≤ V1 ≤ 3.85V

4039 **PW04** **WB DAC -ve Full Scale Check**

Set: WBV DAC to Full Scale (3.66V) using Serial Bus. ACHF-L active by Serial Bus (TTU input connected to front panel socket). Enable DCFB- by HFD1-H.
Pathway: WBV DAC output 'OUT1' (A-D pcb U201-1) via J107-4 to WBV pcb J201-10 to U201-2. From U201-1 via U203-6/7 enabled, to J201-2 'WB_AC'. A-D pcb J107-3 to U401-4 A-D MUX.
Measure: DC Level of WB_AC via A-D (checks performance of DAC inverter for full output swing).

Test Limits -V1 ± 100mV [Where V1 is the stored value from the test for PW03.]

4040 **PW05** **WB DAC +3.5V Check**

Set: WBV DAC to 3.5V using Serial Bus. ACHF-L active by Serial Bus (TTU input connected to front panel socket). Enable DCFB+ by HFD0-H.
Pathway: WBV DAC output 'OUT1' (A-D pcb U201-1) via J107-4 to WBV pcb J201-10 to U201-2. From U201-1 to U201-6; U201-7, via U203-3/2 enabled, to J201-2 'WB_AC'. A-D PCB J107-3 to U401-4 A-D MUX.
Measure: DC Level of WB_AC via A-D (checks performance of DAC output at 3.5V).
Store: Measured reading as 'V2'

Test Limits 3.31V ≤ V2 ≤ 3.69V

4041 PW06 WB DAC -3.5V Check

Set: WBV DAC to 3.5V using Serial Bus. ACHF-L active by Serial Bus (TTU input connected to front panel socket). Enable DCFB- by HFD1-H.

Pathway: WBV DAC output 'OUT1' (A-D pcb U201-1) via J107-4 to WBV pcb J201-10 to U201-2.
From U201-1 via U203-6/7 enabled, to J201-2 'WB_AC'.
A-D pcb J107-3 to U401-4 A-D MUX.

Measure: DC Level of WB_AC via A-D (checks performance of DAC inverter at-3.5V).

Store: Measured reading as 'V3'

Test Limits $-V2 - 10mV \leq V3 \leq -V2 + 10mV$ [Where V2 is the stored value from the test for PW05.]

4042 PW07 WB DC Switch +ve Check

Set: WBV DAC to 3.5V using Serial Bus. ACHF-L inactive by Serial Bus (TTU input connected to chopper output). Enable DCFB+ by HFD0-H.

Pathway: WBV DAC output 'OUT1' (A-D pcb U201-1) via J107-4 to WBV pcb J201-10 to U201-2.
From U201-1 to U201-6; U201-7, via U203-3/2 enabled, to J201-2 'WB_AC'.
A-D PCB J107-3 to U401-4 A-D MUX.

Measure: DC Level of WB_AC via A-D (checks the loading effect of the DC Switch Buffer and associated switch circuits on the DAC output, assuming that the signal path has been connected).

Test Limits $V2 - 1mV \leq WB\_AC \leq V2 + 1mV$ [Where V2 is the stored value from the test for PW05.]

4043 PW08 WB DC Switch -ve Check

Set: WBV DAC to 3.5V using Serial Bus. ACHF-L inactive by Serial Bus (TTU input connected to chopper output). Enable DCFB- by HFD1-H.

Pathway: WBV DAC output 'OUT1' (A-D pcb U201-1) via J107-4 to WBV pcb J201-10 to U201-2.
From U201-1 via U203-6/7 enabled, to J201-2 'WB_AC'.
A-D pcb J107-3 to U401-4 A-D MUX.

Measure: DC Level of WB_AC via A-D (checks the loading effect of the DC Switch Buffer and associated switch circuits on the DAC output, assuming that the signal path has been connected).

Test Limits $V3 - 1mV \leq WB\_AC \leq V3 + 1mV$ [Where V3 is the stored value from the test for PW06.]

4044 PW09 WB TTU DC 3.5V Check

Set: WBV DAC to 3.5V using Serial Bus. ACHF-L inactive by Serial Bus (TTU input connected to chopper output). DCFB+ and DCFB- Disabled by both HFD1-H and HFD0-H inactive, enabling U203-11/10 (TTU amplifier output to the A-D multiplexer).

Pathway: WBV DAC output 'OUT1' (A-D pcb U201-1) via J107-4 to WBV pcb J201-10 to U201-2.
From U201-1 to U201-6 and to DC_CHOP via U204-3/2; U201-7 to DC_CHOP via U204-6/7.
DC_CHOP to U102-3; U102-6 via Q108, Q109 and Q111 to the TTU A101. TTU output 'TTOP' to U205-3; U205-6 via U203-11/10 to J201-2 'WB_AC'.
A-D PCB J107-3 to U401-4 A-D MUX.

After 12 secs settling time:

Measure: DC Level of the TTU amplifier output at WB_AC, via the A-D (checks the output of the DC Switch; the AC Switch 'off' state; the TTU and TTU amplifier performance).

Test Limits $4.67V \leq$ TTU amp o/p $\leq 7.47V$

2.7.6.3 Wide Band (WBV) Tests (Contd.)

4045 PW10 WB TTU DC 1.0V Check

Set: WBV DAC to 1.0V using Serial Bus. ACHF-L inactive by Serial Bus (TTU input connected to chopper output). DCFB+ and DCFB- Disabled by both HFD1-H and HFD0-H inactive, enabling U203-11/10 (TTU amplifier output to the A-D multiplexer).

Pathway: WBV DAC output 'OUT1' (A-D pcb U201-1) via J107-4 to WBV pcb J201-10 to U201-2.
From U201-1 to U201-6 and to DC_CHOP via U204-3/2; U201-7 to DC_CHOP via U204-6/7.
DC_CHOP to U102-3; U102-6 via Q108, Q109 and Q111 to the TTU A101. TTU output 'TTOP' to U205-3; U205-6 via U203-11/10 to J201-2 'WB_AC'.
A-D PCB J107-3 to U401-4 A-D MUX.

After 12 secs settling time:

Measure: DC Level of the TTU amplifier output at WB_AC, via the A-D (checks the linearity of the DC Switch, the TTU and TTU amplifier).

Test Limits 0.41V ≤ TTU amp o/p ≤ 0.69V

4046 PW11 WB TTU DC 0V Check

Set: WBV DAC to 0V using Serial Bus. ACHF-L inactive by Serial Bus (TTU input connected to chopper output). DCFB+ and DCFB- disabled by both HFD1-H and HFD0-H inactive, enabling U203-11/10 (TTU amplifier output to the A-D multiplexer).
K101 on A-D pcb and K101 on WBV pcb energized by TESTD and 100mVHF-H signals respectively. This connects the WBV input to +5V in the A-D pcb to test that Q111/Q112 are correctly switched off.

Pathway: WBV DAC output 'OUT1' (A-D pcb U201-1) via J107-4 to WBV pcb J201-10 to U201-2.
From U201-1 to U201-6 and to DC_CHOP via U204-3/2; U201-7 to DC_CHOP via U204-6/7.
DC_CHOP to U102-3; U102-6 via Q108, Q109 and Q111 to the TTU A101. TTU output 'TTOP' to U205-3; U205-6 via U203-11/10 to J201-2 'WB_AC'.
A-D PCB J107-3 to U401-4 A-D MUX.

After 12 secs settling time:

Measure: DC Level of the TTU amplifier output at WB_AC, via the A-D. (Checks the offset performance of the DC Switch, the TTU and TTU output amplifier. Also checks the isolation performance of the AC Switch.)

Test Limits | TTU amp o/p | ≤ 100mV

4047 PW12 WB TTU AC 0V Check

Set: WBV DAC to 3.5V using Serial Bus to test that Q109/Q110 are correctly switched off. ACHF-L active by Serial Bus (TTU input connected to front panel input). DCFB+ and DCFB- disabled by both HFD1-H and HFD0-H inactive, enabling U203-11/10 (TTU amplifier output to the A-D multiplexer).

Pathway 1: 0V_14 through WBV pcb 50Ω input termination to TTU (A101) input. TTU output 'TTOP' to U205-3; U205-6 via U203-11/10 to J201-2 'WB_AC'.
A-D PCB J107-3 to U401-4 A-D MUX.

Pathway 2: WBV DAC output 'OUT1' (A-D pcb U201-1) via J107-4 to WBV pcb J201-10 to U201-2.
From U201-1 to U201-6 and to DC_CHOP via U204-3/2; U201-7 to DC_CHOP via U204-6/7.
DC_CHOP to U102-3; U102-6 disconnected from A101 input by Q109 and Q110 turned off.

Measure: DC Level of the TTU amplifier output at WB_AC, via the A-D. (Checks the offset performance of the AC Switch. Also checks the isolation performance of the DC Switch.)

Test Limits 0V ≤ | TTU amp o/p | ≤ 100mV

4048 PW13 Not used

4049 PW14 A-to-D WB Path Check

Set: WBV DAC to 0V using Serial Bus. ACHF-L active by Serial Bus (TTU input connected to front panel input). DCFB+ and DCFB- disabled by both HFD1-H and HFD0-H inactive, enabling U203-11/10 (TTU amplifier output to WB_AC).

Pathway: K101 on A-D pcb and K101 on WBV pcb energized by TESTD and 100mVHF-H signals respectively. This connects the WBV input to +5V in the A-D pcb providing an input to TTU of +1V. Same 1V signal in A-D pcb sent via J121-3 and J121-1 to Hi Acc ACV pcb J31-3 and J31-1, to U101-2 (Via K101-4/3) and U101-3.
U101-6 output via K101-7/2 and Q104 as AC_SENSE_SIG to J30-1, A-D PCB J120-1 to U401-7 A-D MUX.

Measure: DC Level of AC_SENSE_SIG, via the A-D.

Store: Measured reading as 'V4'

Test Limits AC_SENSE_SIG ≤ -0.900V

(If AC_SENSE_SIG > -0.900V | , then the 50Ω input is possibly short-circuit, or K101 on the High Acc. ACV pcb is in the wrong state or faulty.)

4050 PW15 WB Input Path Check

Set: WBV DAC to 0V using Serial Bus. ACHF-L active by Serial Bus (TTU input connected to front panel input). DCFB+ and DCFB- disabled by both HFD1-H and HFD0-H inactive, enabling U203-11/10 (TTU amplifier output to the A-D multiplexer).

Pathway: K101 on A-D pcb and K101 on WBV pcb energized by TESTD and 100mVHF-H signals respectively. This connects the WBV input to +5V in the A-D pcb providing an input to TTU (A101) of +1V.
TTU output 'TTOP' to U205-3; U205-6 via U203-11/10 to J201-2 'WB_AC'.
A-D PCB J107-3 to U401-4 A-D MUX.

Measure: DC Level of the TTU amplifier output at WB_AC, via the A-D. .(Checks the AC signal path and the AC switch on the WB pcb.)

Test Limits 0.41V ≤ TTU amp o/p ≤ 0.69V

4051 PW16 WB Input Z, DC Chan Check

Set: WBV DAC to 0V using Serial Bus. ACHF-L inactive by Serial Bus (TTU input connected to chopper output). DCFB+ and DCFB- disabled by both HFD1-H and HFD0-H inactive, enabling U203-11/10 (TTU amplifier output to WB_AC).

Pathway: K101 on A-D pcb and K101 on WBV pcb energized by TESTD and 100mVHF-H signals respectively. This connects the WBV input to +5V in the A-D pcb providing an input to Q111 of +1V (but Q111 turned off). Same 1V signal in A-D pcb sent via J121-3 and J121-1 to Hi Acc ACV pcb J31-3 and J31-1, to U101-2 (Via K101-4/3) and U101-3.
U101-6 output via K101-7/2 and Q104 as AC_SENSE_SIG to J30-1, A-D PCB J120-1 to U401-7 A-D MUX.

Measure: DC Level of AC_SENSE_SIG, via the A-D.
(Checks input-impedance compensation circuit Q105/R136/R137 for DC channel mode)

Test Limits V4 - 1mV ≤ AC_SENSE_SIG ≤ V4 + 1mV

4052 PW17 WB 100mV Path Check

Set: WBV DAC to 0V using Serial Bus. ACHF-L active by Serial Bus (TTU input connected to front panel input). DCFB+ and DCFB- disabled by both HFD1-H and HFD0-H inactive, enabling U203-11/10 (TTU amplifier output to WB_AC).

Pathway: K101 on A-D pcb energized by TESTD active, and and K101 on WBV pcb unenergized by 100mVHF-H inactive. On the WB pcb, this connects the attenuator in the output of U101 to +5V via 200Ω in the A-D pcb setting the WBAC_HI line on th A-D pcb to +2.4V. This is sent via J121-3 and J121-1 to Hi Acc ACV pcb J31-3 and J31-1, to U101-2 (Via K101-4/3) and U101-3.
U101-6 output via K101-7/2 and Q104 as AC_SENSE_SIG to J30-1, A-D PCB J120-1 to U401-7 A-D MUX.

Measure: DC Level of AC_SENSE_SIG, via the A-D.

Test Limits -3.1V ≤ AC_SENSE_SIG ≤ -1.7V

(If AC_SENSE_SIG < -1.100V , then K101 on WB pcb is either faulty or wrong state, or 50Ω input is > 50Ω.)

SECTION 3 DISMANTLING AND REASSEMBLY

This section contains information and instructions for dismantling the Datron 4920M to PCB level. Reassembly is generally the reverse of dismantling, but where necessary, additional notes are given.

3.1 General Precautions

3.1.1 WARNING

ISOLATE THE INSTRUMENT FROM THE LINE SUPPLY BEFORE ATTEMPTING ANY DISMANTLING OR REASSEMBLY.

3.1.2 CAUTIONS

1. HANDLE THE INSTRUMENT CAREFULLY WHEN PARTIALLY DISMANTLED, TO AVOID SHAKING UNSECURED ITEMS LOOSE.
2. DO NOT TOUCH THE CONTACTS OF ANY PCB CONNECTORS.
3. ENSURE THAT NO WIRES ARE TRAPPED WHEN FITTING COMPONENTS, ASSEMBLIES OR COVERS.
4. DO NOT ALLOW WASHERS, NUTS, ETC. TO FALL INTO THE INSTRUMENT.

3.2 General Mechanical Layout

Assembly Drawings in Volume 2, Section 11, pages 11.1-1 to 11.1-8; show how the 4920M is broken down into sub-assemblies.

3.2.1 Front Panel

The Front Panel layout is illustrated in the User's Handbook, Section 3, Page 3-1.

Two fixed N-type plugs are provided at the left side of the panel, for connection to the source being measured.

Two displays are mounted side-by-side. The left-hand display shows the measurement reading, also providing activity symbols for the keys beneath the screen. The right-hand display presents menus as selected by the menu keys below it, showing instrument current-status information.

Two banks of pushbutton switches are provided to control the instrument's operation. For each switch, some indication of the action of pressing the switch is given on one of the two displays.

The line power is turned on and off by a toggle pushbutton on the extreme right side of the Front Panel.

3.2.2 Rear Panel

The Rear Panel Layout is illustrated and described in the User's Handbook, Section 2, Page 2-3.

Selection of Line Voltage is described in the User's Handbook, Section 2, Page 2-4: **'Preparation for Operation'**.

Electrical Connectors, are described in the User's Handbook, Section 2, Page 2-8: **'Connectors and Pin Designations'**.

3.3 Location and Access

3.3.1 External Construction

The front and rear panels are joined by two side extrusions running from front to rear. These extrusions provide slots for the handles or rack mounting 'ears'. Top and bottom covers are fitted by sliding them forward along the extrusions, then each is secured by two captive spring-loaded screws to the rear panel. The bottom cover carries the tilt-stand and four rubber feet. Ground screening of the covers is provided by aluminium plates fitted to the inside of the covers; the main ground connections being made to the rear panel through the securing screws.

3.3.2 Internal Construction

Inside the covers, mechanical strength is provided by the two side extrusions, separated and secured by two cross supports - the rear panel plate, and a similar plate at the front - which together form a rigid box-section. An internal cross support divides the interior of the instrument into front and rear partitions:

Interior Partitions

- The **Rear Partition** is occupied by a sub-chassis screwed to both the rear panel metalwork and the internal cross support. Mains (Line) and Low-Voltage transformers are secured to the underside, and external electrical connections pass through the rear of the sub-chassis.

  On the upper sub-chassis, nylon slides locate the Digital PCB Assembly, which fits at the front into polycarbonate mounts on the main cross support, with screws securing the assembly to the rear panel metalwork. A Mylar sheet glued to the top of the sub-chassis provides insulation for the joints on the underside of the digital assembly. External electrical connections to the assembly pass through the rear panel metalwork, which is also used as an additional heatsink for four transistors.

- The **Front Partition** contains the metal Shield Assembly, attached by a total of five polycarbonate insulators to the front panel metalwork and internal cross support. The assembly is divided into upper and lower spaces by a horizontal plate.

  Two pcb assemblies are mounted on top of the Shield: the Wide Band AC PCB Assembly, in its screening case, is fitted on the left; the A-D / Control PCB Assembly is on the right. The High Accuracy AC PCB Assembly is mounted on the underside. All three assemblies are screwed into nuts captive in the shield plate.

- **Connecting Cables** between the various assemblies pass through cut-outs in the metalwork, and are loomed and secured where necessary.

Front Extension

The instrument extends forward from the main box section to accomodate the front panel components. Externally it is enclosed by a structural-foam bezel, complete with display filters, terminal labels and apertures for the banks of press-button switches. The bezel is secured to the front cross support by two screws and lock washers at each end, which are accessible from the sides of the instrument once the top and bottom covers have been removed.

When the bezel is removed:

- The **Switch Assembly** is mechanically secured to the rear of the bezel, but electrically connected by two cables to two sockets on the component side of the Display PCB. This assembly does not include the Power On/Off switch.

- The **Power On/Off Switch Assembly** is secured by two screws to the rear of the right side extrusion, beneath the sub-chassis. The switch itself is operated by a cranked moulding fitted inside the extrusion slide. The switch action is 'Push On - Push Off'.

  A metal rod in the moulding extends to the front extrusion, where a second cranked moulding connects it to the front panel On/Off pushbutton. The button is a tight push-fit, and not cemented to the moulding, so that it does not prevent the bezel from being removed. The location of the switch is adjusted so that the pushbutton is flush with the bezel when in the 'Off' position, and depressed into the bezel when power is switched 'On'.

- The **Display PCB Assembly** is screwed to the front cross support. It carries the two displays which are viewed through the filters in the bezel. A metal screen on the left end of the assembly shields the signals on the front panel terminations from the high voltage pulses which drive the displays.

- The **'WBV' Precision N-type Input Socket** is mounted on a connector bracket. This is secured by three screws to the front end-plate of the Wide Band PCB Assembly, forming an integral part of it. A rigid coaxial connector passes the input signal from the WBV socket into the assembly.

- The **'ACV' Precision N-type Input Socket** is mounted on a connector bracket, which is secured by four screws to the front cross support. A twisted pair passes the input signal from the ACV socket via the A-D Control Assembly into the High Accuracy PCB Assembly on the underside of the shield plate.

3.4 General Access

- ENSURE THAT POWER IS OFF.
- Heed the General Precautions 3.1.1 and 3.1.2.

If, during a procedure, sufficient access has been obtained, then no further dismantling is required.

3.4.1 Top Cover

- **Removal**

a. Release the two spring-loaded screws holding the cover to the rear panel.

b. Slide the cover to the rear until:
   i. The small locating tongue on the rear of the top ground shield disengages from the rear panel.
   ii. The cover front flange clears the bezel.

c. Lift off the cover.

- **Fitting**

a. Locate the cover on the top rails of the side extrusions, its front flange just behind the bezel.

b. Press down on the cover and slide it forward until:
   i. The cover front flange slides under the bezel.
   ii. The small locating tongue on the rear of the top ground shield engages into the rear panel.

c. Tighten the two spring-loaded screws to secure the cover to the rear panel.

3.4.2 Bottom Cover

- **Removal**

a. With the instrument inverted, release the two spring-loaded screws holding the bottom cover to the rear panel slot.

b. Slide the cover to the rear until:
   i. The small locating tongue on the rear of the bottom ground shield disengages from the rear panel.
   ii. The cover front flange clears the bezel.

c. Lift off the cover.

- **Fitting**

a. With the instrument inverted, locate the bottom cover on the bottom rails of the side extrusions, its front flange just behind the bezel.

b. Press down on the cover and slide it forward until:
   i. The cover front flange slides under the bezel.
   ii. The small locating tongue on the rear of the bottom ground shield engages into the rear panel slot.

c. Tighten the two spring-loaded screws which secure the cover to the rear panel.

3.4 General Access (Contd.)

3.4.3 Front Bezel

- Remove top and bottom covers: 3.4.1 and 3.4.2.

- **Removal**
  (Page 11.1-1, DA400927 Sh. 1)

a. Remove the four M2.5 x 6mm Pozipan screws holding the bezel to the side extrusions, each with its two spring washers.

b. Gently withdraw the bezel from the body of the instrument, taking care to retain the power switch key cap, which is a push fit onto its cranked moulding, and comes away with the bezel. **Do not** attempt to prize the Power key cap out of its recess before removing the bezel - it detaches easily with the bezel. Do not strain the two ribbon cables connecting the Switch PCB to the Display PCB.

- **Fitting**

Reverse the removal procedure, consulting the reference drawings at each stage. Be careful not to trap any wiring. Tighten down the screws and make a final inspection to ensure that the ribbon cable and mechanical elements are correctly fitted and secured.

3.4.4 Rear Panel Assembly

N.B. *For most purposes it should not be necessary to remove the Rear Panel Assembly. However, it is necessary when the Digital PCB Assembly is to be taken out. It can be easier to remove the Rear panel and Digital board together, separating the two later, than to remove the panel first. Two procedures are given, the first to remove the Rear Panel on its own (in this sub-section), and the second to remove the Digital assembly (in sub-section 3.5.1).*

- Remove top and bottom covers: 3.4.1 and 3.4.2.

- **Removal of Rear Panel Only**
  (Facing page 11.1-3, DA400928 Sh. 1)

a. Remove the eight M3 x 8mm Pozipan screws which attach the Rear Panel to the sub-chassis and digital assembly.

b. Remove the four M3 x 8mm Pozi-countersunk screws which secure the Rear Panel to the side extrusions.

c. Gently ease the rear panel and attached corner blocks away from the body of the instrument and remove.

- **Fitting**

a. Offer up the rear panel to the body of the instrument, locating the corner-block spigots into the channels of the side extrusion.

b. Reverse the removal procedure, consulting the reference drawings at each stage. Be careful not to trap any wiring. Make a final inspection to ensure that the wiring is correctly fitted and secured.

3.5 Sub-Assembly Removal and Fitting

3.5.1 Digital PCB Assembly

- Remove top and bottom covers: 3.4.1 and 3.4.2.
- Stand the instrument in its normal upright position.

3.5.1.1 Removal of combined Rear Panel and Digital PCB Assembly

a. Carefully remove the three 3M ribbon connectors from PL1, PL2 and PL3 on the right front corner of the Digital Assembly.
(DA400933 sheet 2: Sect 11 facing page 11.3-1).
Note: Each 3M ribbon connector has a rectangular key, which locates into a recess in the fixed socket shroud, leaving a narrow slot into which a small screwdriver blade can be inserted and twisted to lever off the connector.

b. Carefully remove the three Molex connectors from PL4, PL5 and PL6 on the right end of the Digital Assembly.
(DA400933 sheet 2: Sect 11 facing page 11.3-1).

c. Remove the three M3 x 8mm Pozipan screws which attach the Rear Panel to the sub-chassis.
(DA400928 sheet 1: Sect 11 facing page 11.1-3)

d. Remove the four M3 x 8mm Pozi-countersunk screws which secure the Rear Panel to the side extrusions.
(DA400928 sheet 1: Sect 11 facing page 11.1-3)

e. Gently ease the rear panel and digital assembly away from the body of the instrument. Carefully slide the two to the rear, and remove.

- **Fitting**

a. Locate the Digital Assembly PCB into the nylon slides fitted to the sub-chassis.

b. Reverse the removal procedure, consulting the reference drawings at each stage. Slide the combination forward, until the digital assembly is fully home between the tongues of the three polycarbonate mounts on the cross support. Be careful not to trap any wiring.

c. Make a final inspection to ensure that the wiring, ribbon cables and sockets are correctly fitted and secured.

3.5.1.2 Separating the Removed Rear Panel and Digital PCB Assembly

- **Separation**

  Remove the five M3 x 8mm Pozipan screws which attach the Rear Panel to the Digital Assembly, and carefully separate the two.
  (DA400928 sheet 1: Sect 11 facing page 11.1-3)

- **Recombination**

  Reverse the separation procedure.

3.5 Sub-Assembly Removal and Fitting (Contd.)

3.5.2 Display PCB

- Remove top and bottom covers: 3.4.1 and 3.4.2.
- Remove the Front Bezel: 3.4.3.

- **Removal**
  (DA400928 sheet 1: Sect 11 facing page 11.1-3)

a. Disconnect the two eight-way ribbon connectors from PL22 and PL23 (From the Switch Assembly in the Bezel) on the front of the Display PCB. Note the correct positions for later return
(See also DA400744 sheet 1: Sect 11 facing page 11.2-2; and DA400739 sheet 1: Sect 11 facing page 11.2-1)

b. Remove the Bezel and Switch Assembly.

c. At the right end of the display assembly, pull the cranked moulding off the Power Switch operating rod.

d. Disconnect the two 3M ribbon connectors from PL20 and PL21 on the front of the Display PCB.
Note: The 3M ribbon connector has a rectangular key, which locates into a recess in the fixed plug shroud, leaving a small slot into which a small screwdriver blade can be inserted and twisted to lever off the socket easily.

e. Remove the three M3 x 8mm Pozipan screws which attach the Display Assembly to standoffs on the Front Panel metalwork.

f. Disengage the Display Assembly from the four black retainers on the top of the front panel metalwork, and carefully remove.

- **Fitting**

Reverse the removal procedure, consulting the reference drawings at each stage. Be careful not to trap any wiring. Make a final inspection to ensure that the wiring and ribbon cables are correctly fitted and secured.

3.5.3 Front Panel Switch PCB Assembly

- Remove top and bottom covers: 3.4.1 and 3.4.2.
- Remove the Front Bezel: 3.4.3.

- **Removal**
  (DA400931 Sh. 1, Sect 11 page 11.1-6)

a. Lay the Bezel face down, so that the rear of the Switch Assembly is accessible.

b. Remove the two M2.5 x 6mm Pozipan screws, each with its shakeproof and plain washer, which attach the assembly to the bezel at the right end of the switch assembly.

c. Remove the two M2.5 x 12mm Pozipan screws, each with its shakeproof and plain washer, which attach the assembly to the bezel through the support bar running across the rear of the assembly.

d. Carefully lift the switch assembly, complete with key caps, from the bezel. The key caps should slide easily through the two apertures in the bezel.

- **Fitting**

Ensure that the key caps are correctly fitted. Reverse the removal procedure, consulting the reference drawings at each stage. Make a final inspection to check that the key caps are correctly oriented.

3.5.4 'ACV' N-Type Input Socket

- Remove top and bottom covers: 3.4.1 and 3.4.2.
- Remove the Front Bezel: 3.4.3.
- **Removal**

(Facing page 11.1-1, Drawing DA400927 Sh. 1)
(Facing page 11.1-3, Drawing DA400928 Sh. 1)
(Facing page 11.4-1, Drawing DA400936 Sh. 1)

a. Stand the instrument in its normal upright position.

b. Disconnect the Molex connector from J102 at the left front of the A-D assembly (Upper half of instrument - twisted pair).

c. Remove four M3 Pozipan screws which attach the socket bracket to the front cross support.

d. Withdraw the bracket and socket from the instrument, carefully feeding the twisted pair and Molex connector through the gap between the front of the shield and the front cross support.

e. The N-type socket connector assembly can now be removed from the bracket by unscrewing the socket nut.

- **Fitting**

a. Reverse the removal procedure, consulting the reference drawings at each stage. Be careful to route and reconnect the twisted pair correctly.

3.5.5 A-D / Control PCB Assembly

- Remove top cover: 3.4.1.
- **Removal**

(Page 11.1-3, Drawing DA400928 Sh. 2)
(Facing page 11.4-1, Drawing DA400936 Sh. 1)

a. Stand the instrument in its normal upright position.

b. Disconnect the Molex connector from J102 at the left front corner of the A-D assembly.
(Input connection - black/white twisted pair.)

c. Disconnect the Molex connector from J131 at the left front corner of the A-D assembly (connection to AC Wideband Assembly).

d. Release the spring clip which retains the 3M ribbon connector in PL3 at the right front corner of the Digital Assembly, by pushing it over away from the ribbon. Disconnect the connector by lifting it clear of the fixed socket shroud. Release the ribbon cable from its housing on the cross chassis. (This cable is soldered at the A-D / Control Assembly end as J110.)

e. Release the spring clips which retain the 3M ribbon connectors in J105 and J107 at the left rear of the A-D assembly, by pushing them over away from the ribbon. Disconnect the connectors by lifting them clear of the socket shrouds.
Note: Each 3M ribbon connector has a rectangular key, which locates into a recess in the fixed socket shroud underneath the ribbon, leaving a narrow slot into which a small screwdriver blade can be inserted and twisted to lever off the connector.

f. Disconnect the Molex connector from J103 on the A-D / Control Assembly.

g. Disconnect the Molex connectors from J120/121/122 at the left front corner of the A-D / Control Assembly (High Accuracy ACV Assembly connections).

h. Release the A-D / Control Assembly by removing the five M3 x 6 Pozipan screws, each with its wavy washer.

j. Gently lift the A-D / Control Assembly out of the instrument, taking care not to damage any cables or components, and remove.

- **Fitting**

Reverse the removal procedure, consulting the reference drawings at each stage. Be careful not to trap any wiring. Make a final inspection to ensure that the cable plugs are connected to the correct sockets.

3.5 Sub-Assembly Removal and Fitting (Contd.)

3.5.6 AC Wideband Assembly

N.B. Removal of this 'Sub-assembly' is limited to taking the screened box out of the instrument. Further disassembly should not be attempted unless the necessary equipment is available to recalibrate the WBV function.

- Remove top cover: 3.4.1.

- **Removal**

(Page 11.1-3, Drawing DA400928 Sh. 2)
(Facing page 11.4-1, Drawing DA400936 Sh. 1)
(Facing page 11.7-2, Drawing DA400939 Sh. 1)

a. Stand the instrument in its normal upright position.

b. Disconnect the Molex connector from J131 at the front left of the A-D assembly (connection to WBV PCB Assembly). Release the cable from its clip on the front panel.

c. Release the spring clip which retains the 3M ribbon connector in J107 at the left rear of the A-D assembly, by pushing it over away from the ribbon. Disconnect the connector by lifting it clear of the fixed socket shroud. Release the ribbon cable from its clip on the chassis.
Note: Each 3M ribbon connector has a rectangular key, which locates into a recess in the fixed socket shroud underneath the ribbon, leaving a narrow slot into which a small screwdriver blade can be inserted and twisted to lever off the connector.
Release the ribbon cable from its clip on the center panel.

d. Release the AC Wideband Assembly from the center panel by removing the six M3 x 6 Pozipan screws, each with its shakeproof washer.

e. Gently move the assembly to the rear to extract the integral WBV precision 'N' type receptacle and mounting bracket from its housing in the Bezel. Lift the assembly out of the instrument, taking care not to damage any cables or components, and remove.

f. Remove the two 4-40 x 3/8 Pozipan screws,each with its shakeproof washer and plain washer, securing the D-type ribbon plug to J201 at the rear of the AC Wideband Assembly. Disconnect and remove the cable and socket from J201. If the assembly is to be returned for service, retain the complete ribbon cable, screws and washers for fitting to the replacement assembly.

- **Fitting**

Reverse the removal procedure, consulting the reference drawings at each stage. Be careful not to trap any wiring. Ensure that the WBV socket fits correctly into its hole in the bezel, before finally tightening the assembly down to the center panel. Make a final inspection to ensure that the cable sockets are correctly connected and secured.

3.5.7 High Accuracy ACV Preamplifier

N.B. Removal of this 'Sub-assembly' is limited to taking the complete PCB Assembly out of the instrument. Further disassembly should not be attempted unless the necessary equipment is available to recalibrate the ACV function.

- Remove bottom cover: 3.4.2.

- **Removal**

(Page 11.1-4, Drawing DA400928 Sh. 3)
(Facing page 11.5-1, DA400938 Sh. 1)

a. Ensure that the instrument is inverted.

h. Release the Preamp PCB Assembly by removing the five M3 x 6 Pozipan screws, each with its wavy washer, which secure it to the High Accuracy ACV PCB Assembly.

j. Holding the Preamp PCB Assembly by its left and right ends, and keeping it parallel with the ACV PCB beneath, gently lift the assembly to disconnect its three connector sockets: P34; P35; P36 from their plugs on the ACV PCB. Lift the assembly out of the instrument, taking care not to damage any cables or components, and remove.

- **Fitting**

Reverse the removal procedure, consulting the reference drawings at each stage. Becareful not to trap any wiring.

3.5.8 High Accuracy ACV PCB Assembly

N.B. Removal of this 'Sub-assembly' is limited to taking the complete PCB Assembly out of the instrument. Further disassembly should not be attempted unless the necessary equipment is available to recalibrate the ACV function.

- Remove bottom cover: 3.4.2.
- Remove the High Accuracy Preamplifier Assembly: 3.5.7.
- **Removal**

(Page 11.1-4, Drawing DA400928 Sh. 3)
(Page 11.6-1, DA400937 Sh. 1)

a. Ensure that the instrument is inverted.

b. Release the spring clip which retains the 3M ribbon connector in J33 at the rear of the assembly, by pushing it over away from the ribbon. Disconnect the socket by lifting it clear of the fixed socket shroud.
Note: Each 3M ribbon connector has a rectangular key, which locates into a recess in the fixed socket shroud opposite the ribbon, leaving a narrow slot into which a small screwdriver blade can be inserted and twisted to lever off the connector.

c. Disconnect the Molex connectors from J30/31/32 at the left front of the assembly.

h. Release the assembly by removing the seven M3 x 6 Pozipan screws, each with its wavy washer, which secure it to the Center Panel.

n. Gently lift the assembly out of the instrument, taking care not to damage any cables or components, and remove.

- **Fitting**

Reverse the removal procedure, consulting the reference drawings at each stage. Becareful not to trap any wiring.

3.6 Transformer Assemblies

3.6.1 Mains Transformer Assembly *(This Assembly includes the Power Switch and Voltage Selector Switch)*

N.B. To fit a mains transformer after removal, an M4 torque wrench capable of setting to 4Nm is required. Two 'Tyrap' cable ties will be required (Datron part No.: 590013).

- Remove top and bottom covers: 3.4.1 and 3.4.2.
- Remove the Rear Panel: 3.4.4.

- **Removal**

(Facing page 11.1-4, Drawing DA400928 Sh. 3)
(Page 11.1-4, Drawing DA400929 Sh. 1)
(Facing page 11.1-6, Drawing DA400929 Sh. 4)
(Facing page 11.1-8, Drawing DA400749 Sh. 1)
(Facing page 11.3-2, Drawing DA400933 Sh. 1)

a. Ensure that the instrument is inverted.

b. Identify the Mains Transformer (the larger of the two), Power Switch and Voltage Selector Switch, in the right end of the sub-chassis at the rear of the instrument.

c. Identify the **green/yellow** ground bonding lead from the mains transformer to the bonding point between the power input plug and the power fuse, on the sub-chassis.

d. Remove the nut from the bonding point and remove the green/yellow lead identified in (c) above. Replace the nut to retain the bonding braid.

e. After noting how they are positioned, cut the two 'TYRAP' cable ties that hold the transformer wiring.

f. Turn the instrument to its upright position and disconnect the Molex socket of the mains transformer cable from PL5 (A & B) on the Digital PCB Assembly. Carefully feed the cable and socket back through the gap at the end of the sub-chassis, to the same side as the mains transformer.

g. Return the instrument to its inverted position.

h. Remove the two M4 nylock nuts and plain washers which attach the Mains Transformer to the sub-chassis studs.

j. Tip the instrument to stand on its right side and remove the mains transformer, laying it down on the bench so that the remaining wiring is not strained.

k. Identify the Power Switch assembly located in the slider of the right side extrusion. Remove two hex socket-headed M3 x 6 screws which secure the backplate to a retaining plate inside the extrusion slide.

l. Lever the white operating bar of the power switch out of its cranked slider, and remove the switch.

m. Carefully cut off the heatshrink sleeves at the ends of the blue and brown leads which are connected to the two end tags of the power switch. Note the positions and unsolder the leads from the tags.

n. Identify the Voltage Selector Switch located at the rear of the sub-chassis. Remove two M3 x 8mm Pozi-countersunk screws, nuts and washers which secure the switch to the sub-chassis.

p. Remove the two switches and the Mains Transformer.

- **Fitting**

a. Reverse the dismantling procedure, consulting the reference drawings at each stage. Pay particular attention to the following points:

i. Refer to operation (**m**). Fit new lengths of heatshrink sleeve to the blue and brown leads which were disconnected. Solder the leads to the correct power switch tags. Push the sleeves down to cover the joints completely and shrink to fit.

ii. Stand the instrument on its right side to assist the positioning of the power switch retaining plate correctly in the right extrusion slide. After securing the switch assembly to the retaining plate, ease off the screws and set the switch to Off. Adjust the fore-and-aft position by sliding the whole mechanical assembly until the key cap is flush with the surface of the front panel bezel. Retighten the screws and recheck the key cap alignment.

iii. Take care not to trap any wiring when fitting the transformer.

iv. Using a torque wrench, tighten the transformer securing nuts to 4Nm.

v. Check that the wiring is set in the correct routing, is not trapped, and the connections are mechanically secure.

vi. Tie the cabling together using two new 'TYRAP' cable ties, in the positions noted in operation (**e**).

vii. Carry out a final inspection to ensure that the components are correctly fitted.

3.6.2 Low Voltage Transformer Assembly

N.B. To fit a low voltage transformer after removal, an M4 torque wrench capable of setting to 3Nm is required. Two 'Tyrap' cable ties will be required (Datron part No.: 590013).

- Remove top and bottom covers: 3.4.1 and 3.4.2.

- **Removal**

(Page 11.1-3, Drawing DA400928 Sh. 2)
(Facing page 11.1-4, Drawing DA400928 Sh. 3)
(Page 11.1-4, Drawing DA400929 Sh. 1)
(Facing page 11.1-6, Drawing DA400929 Sh. 4)
(Page 11.1-8, Drawing DA400962 Sh. 1)
(Facing page 11.3-2, Drawing DA400933 Sh. 1)

a. Ensure that the instrument is inverted.

b. Identify the Low Voltage Transformer in the center of the sub-chassis at the rear of the instrument.

c. Turn the instrument to its upright position and disconnect the Molex connectors of the two low voltage transformer cables from PL4 and PL6 on the Digital PCB Assembly.

d. Stand the instrument on its right side. Carefully feed the cables and connectors back through the gap at the end of the sub-chassis, to the same side as the transformer.

e. After noting how they are positioned, cut the two 'TYRAP' cable ties that hold the transformer wiring.

f. Turn the instrument to its upright position and disconnect the Molex connector of the low voltage transformer cable from J103 on the A-D PCB Assembly.

g. Stand the instrument on its right side. Carefully feed the cable and connector back through the cutout in the guard box screen to the same side as the transformer.

h. Return the instrument to its inverted position.

j. Release one end of the perspex cable retainer, by pressing the peg in the center of the plastic split pin and withdrawing the pin. Lift the cable and socket out of the cutout, and re-secure the retainer in position using the split pin.

k. Remove the two M4 nylock nuts and plain washers which attach the Low Voltage Transformer to the sub-chassis studs.

l. Carefully lift out and remove the Low Voltage Transformer, cables and connectors.

- **Fitting**

a. Reverse the dismantling procedure, consulting the reference drawings at each stage. Pay particular attention to the following points:

i. Take care not to trap any wiring when fitting the transformer.

ii. Using a torque wrench, tighten the transformer securing nuts to 3Nm.

iii. Check that the wiring is set in the correct routing, is not trapped, and the connections are mechanically secure.

iv. Tie the cabling together using two new 'TYRAP' cable ties, in the positions noted in operation (e).

SECTION 4 SERVICING

4.1 Routine Servicing

The only routine servicing required under normal conditions is the replacement of the Lithium battery which powers the non-volatile calibration memory.

The calibration requirements after changing the battery are different depending on whether the change was done with power off or with power on. These requirements are summarized in the table below.

Summary *(Refer also to Sub-section 4.2)*

After Battery Change

Servicing and Time Interval	Procedure Section 4	Calibration Required	Calibration Procedure
Change the Internal Battery with Power On			
Not greater than 5 years	4.3	Routine Calibration	User's Handbook Sect 8
Change the Internal Battery with Power Off			
Not greater than 5 years	4.3	Special Calibration Routine Calibration	Sub-sect. 1.4 User's Handbook Sect 8

4.2 Adjustment Following Replacement of PCBs

4.2.1 Removal of Covers - Maintenance Calibration

The high accuracy of this instrument demands that its internal environment remains undisturbed after calibration. After removal of the top or bottom cover, a routine calibration or specification verification may be required (routine calibration is usually simpler - refer to the User's Handbook, Section 8). This is also sufficient for removal and replacement of the following sub-assemblies:

Top Cover, Bottom Cover, Switch PCB, Display PCB,
Mains Transformer, Low Voltage Transformer.
Battery BT1 on the Digital PCB (Changed with power on).

For calibrations required after changing other sub-assemblies, refer to 4.2.2 below.

4.2.2 Routine and Special (Maintenance) Calibrations Required following Change of Sub-Assembly

	Freq Cal	Special Cal ALin	Routine Cal ACV Gain	Routine Cal WBV Gain	Special Cal WLin	Special Cal ACV Flatness	Special Cal WBV 1V Flatness	Special Cal WBV 3V Flatness	Special Cal Filt
Reference to Procedure	**1-6**	**1.4-5**	**User's 8-6**	**User's 8-9**	**1.4.2**	**1.4.4.8**	**1.4.4.8**	**1.4.4.9**	**1.4.3**
Sub-Assembly Changed:									
Battery BT1 in Digital PCB (Changed With Power off)	√	√	√	√	√	√	√	√	√
Digital PCB: Whole PCB	√	√	√	√	√	√	√	√	√
A-D PCB			√	√	√				
High Accuracy AC PCB	√	√	√	√		√	√	√	√
High Accuracy AC Preamp PCB			√			√	√		
AC Wideband PCB				√	√		√	√	

4.3 LITHIUM BATTERY - REPLACEMENT

(Datron Part No. 920228)

FIRST READ THESE NOTES!

- The lithium battery which powers the non-volatile RAM should be changed at or before 5 years from new, and at no greater than 5-year intervals thereafter.
- The following procedures assume that the instrument will remain powered-up during the operations of disconnecting the old battery and connecting the new battery. To ensure memory integrity the soldering iron used must be isolated from line ground (mains earth) by at least 50kΩ.

  Routine calibration will be required *(User's Handbook Section 8)* because of the high accuracy of the instrument, whose internal environment will have been disturbed by removing and replacing the top cover.

  If instrument power does not remain **ON** during the whole of the procedure **4.3.1**, disconnecting the battery will reset the calibration memory to its nominal state. This will require a **Special** Calibration to be carried out *(Section 1.4)* as well as the full Routine Calibration, before the instrument specification can be realized, as calibration data will be corrupted.

  It is therefore strongly recommended that the battery be changed with **Power ON**, immediately prior to a scheduled routine calibration.

4.3.1 Digital Assembly 400933 - Procedure

a. Ensure that power **ON** is selected.

b. Remove the top cover *(Section 3 para. 3.4.1)*.

c. Remove the battery (refer to *Fig. 4.1*):

i. Attach a heatsink to resistor R533 soldered to the battery positive terminal. Unsolder R533 from the battery terminal.

ii. Attach a heatsink to the wire between the negative battery terminal and E502. Unsolder the wire from the battery terminal.

iii. Remove the battery from its clip.

d. Observing correct polarity, reverse the procedure of step (c) to fit a new battery and solder it in.

4.3.2 Return to Use *(Refer also to Sub-section 4.2)*

a. Refit the top cover *(Section 3 para. 3.4.1)*.

b. If the instrument power was turned off during the battery-change procedure, carry out the **Special** Calibration detailed in Section 1.4.

c. Carry out **Full** Routine Recalibration *(User's Handbook Section 8)*.

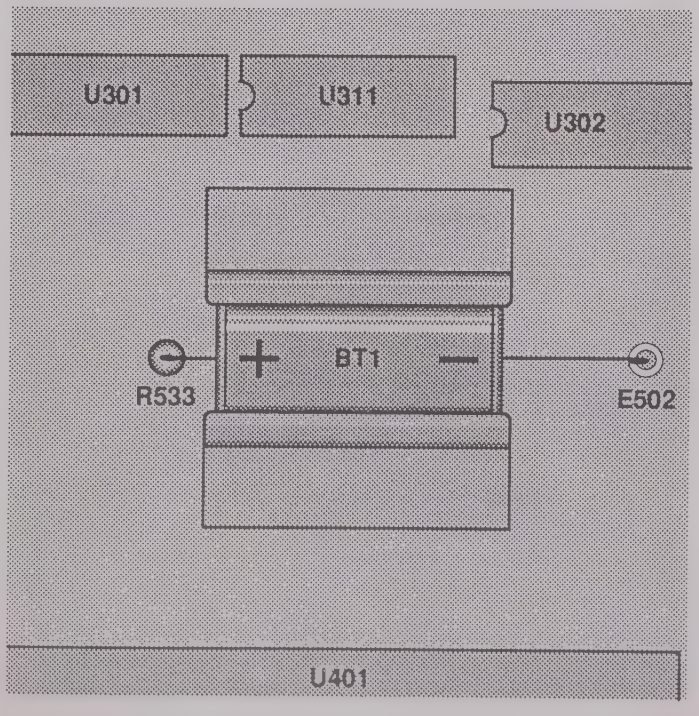
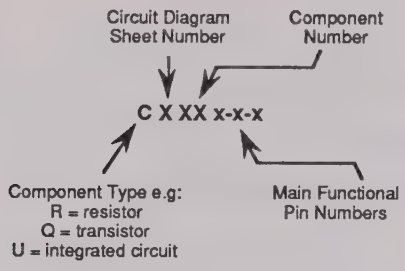


Fig. 4.1 View of Battery from Rear of Instrument

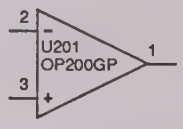
SECTION 5 TECHNICAL DESCRIPTIONS

Note: The technical descriptions in this section use the following conventions to identify individual components and their values:-

Component Identification



Example: Op-amp U2013-2-1 would be found on sheet 2 of the Wideband AC circuit diagram as:



Component Value

In calculations, symbols in the form "C_{xxx}" represent the values of components whose designators are in the form "CXXX".

Example: R_{423} represents the ohmic value of resistor R423.

5.1 Principles of Operation

5.1.1 Simplified Block Diagram

Figure 5.1.1.1 illustrates the main functional blocks and signal flow within the 4920M.

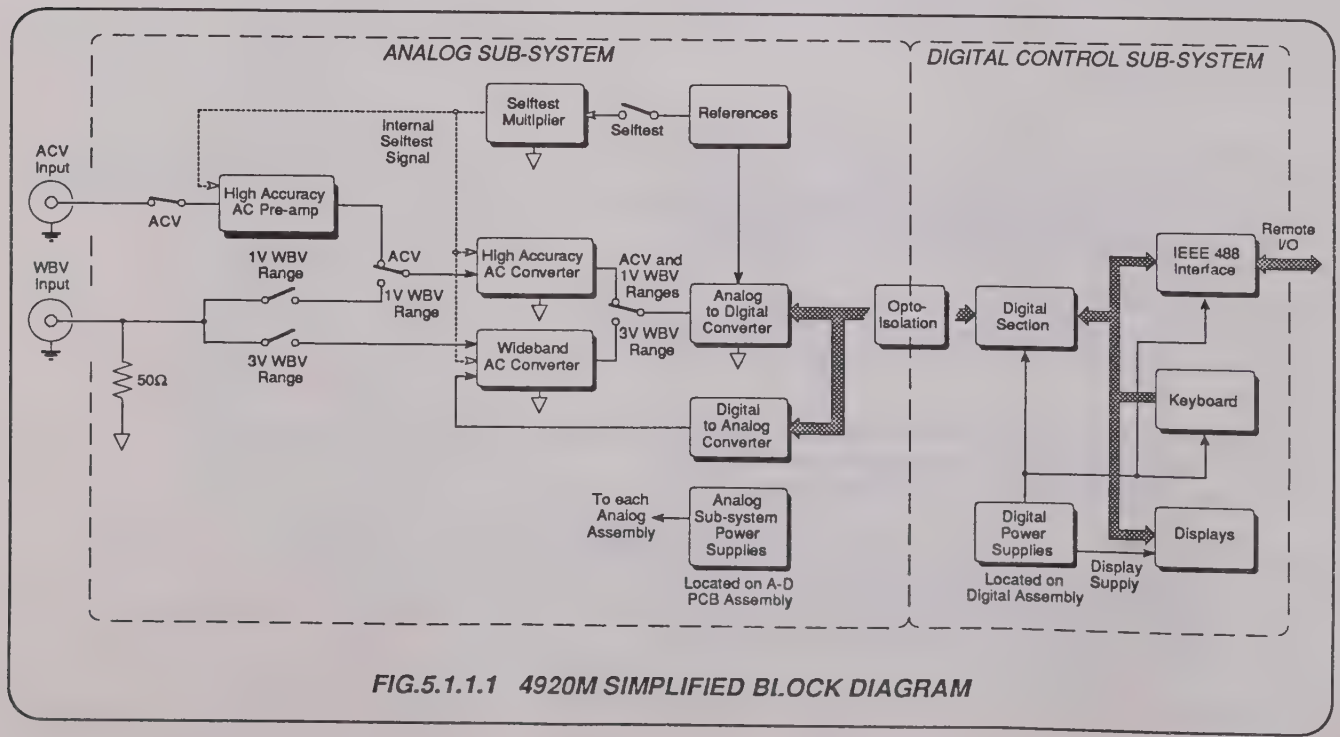


FIG.5.1.1.1 4920M SIMPLIFIED BLOCK DIAGRAM

5.1.2 General Principles

The 4920M Alternating Voltage Measurement Standard is a very high accuracy, true RMS sensing, programmable AC voltmeter designed for calibration and standards laboratory applications. The instrument has two separate inputs – a high accuracy input (ACV input) for high accuracy measurements up to 1000V at frequencies up to 1MHz, and a wideband input (WBV input) for measurements up to 3V at frequencies as high as 20MHz.

5.1.2.1 High Accuracy AC (ACV) Input

The ACV input is used to measure voltages in the range 100mV to 100V over a frequency range of 10Hz to 1MHz, and voltages in the range 100V to 1000V over a frequency range of 10Hz to 100kHz; to very high accuracy (±30 ppm absolute accuracy between 100mV and 100V at frequencies between 40Hz and 20kHz).

The ACV measurement function employs precision AC input attenuators and an electronic RMS detector, to provide the highest possible speed of response.

As part of every measurement cycle the gain of the RMS detector is determined by applying a known AC signal (quasi-sinewave) to it, at an amplitude very close to that of the input value. This technique eliminates linearity errors in the RMS detector, together with time and temperature drifts in the detector's gain.

Three-Measurement Transfer
In practice, each measurement cycle requires three separate measurements to be made by the instrument's A-D converter.

Measurement M1
During the first measurement (**M1**), the ACV input – suitably amplified or attenuated depending on the range selected – is applied to the RMS detector, and the A-D converter measures the DC output of the detector – see Figure 5.1.2.1 (a) opposite. **M1** is the value of the input signal multiplied by the gain of the RMS detector.

$$M1 = K \times V_{ACV(RMS)} \quad \text{.....(1)}$$

While measurement **M1** is being made, the output of the RMS detector is captured and stored by the sample and hold circuit. This stored voltage is subsequently used to define the amplitude of a known AC signal (quasi-sinewave), which is then used to accurately determine the Gain (K) of the RMS detector.

Measurement M2
The second measurement (**M2**) made by the A-D converter is a measurement of the sample and hold circuit's DC output. – see Figure 5.1.2.1 (b).

The output of the sample and hold circuit drives the quasi-sine generator, which produces a fully settled quasi-sinewave output of RMS value M2 ready for the third and final measurement (**M3**).

Measurement M3
M3 is a measurement by the A-D converter of the output of the RMS detector with the quasi-sinewave applied to the detector's input – see Figure 5.1.2.1.(c). The gain of the RMS detector is therefore given by the equation:

$$K = M3/M2 \quad \text{.....(2)}$$

Substituting equation (2) in equation (1) gives:

$$M1 = (M3/M2) \times V_{ACV(RMS)}$$

and therefore:

$$V_{ACV(RMS)} = (M1 \times M2) / M3$$

This equation is evaluated by the 4920M's microprocessor to determine the true RMS value of the ACV input signal from the three A-D converter measurements.

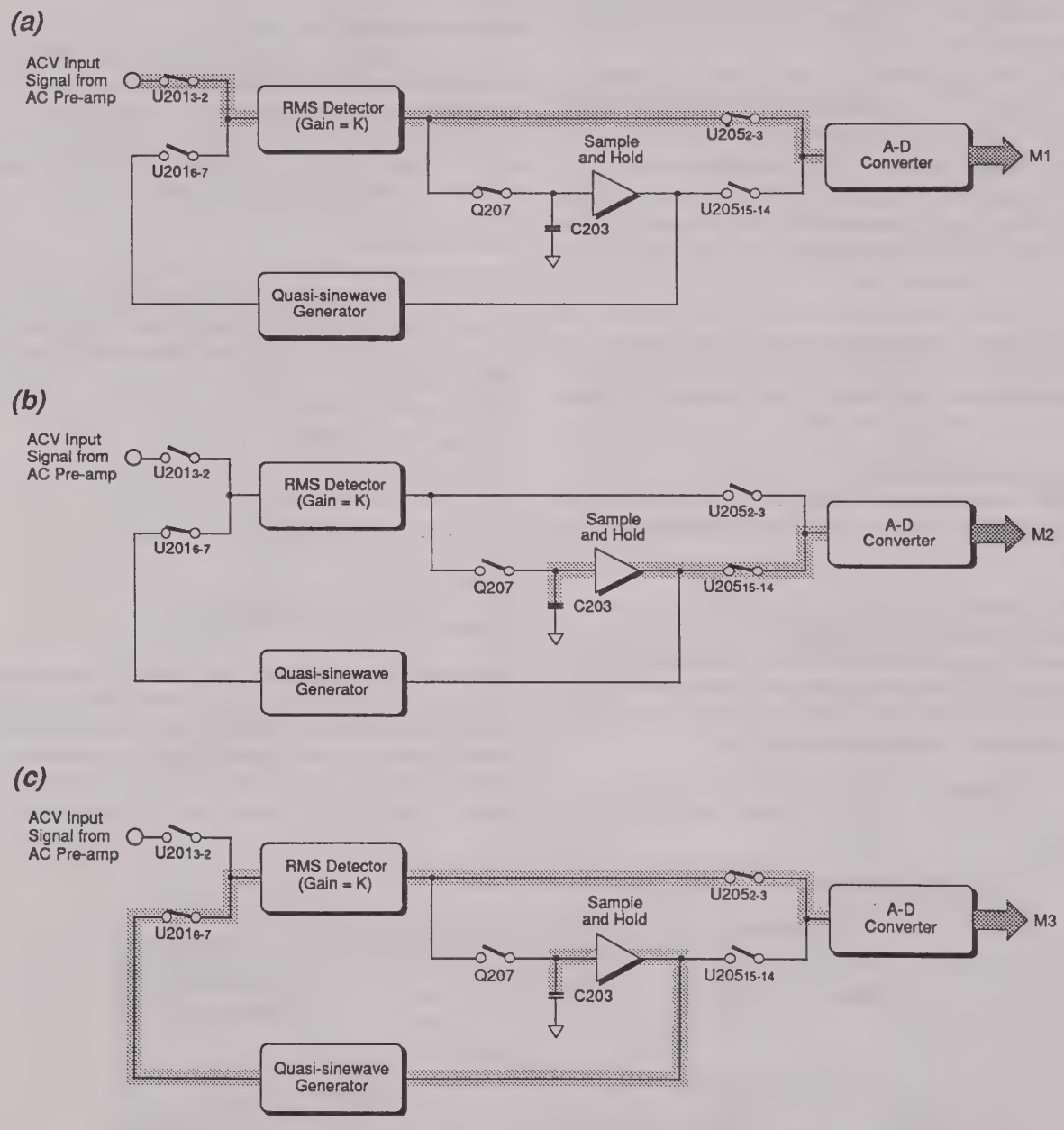


FIG.5.1.2.1 HIGH ACCURACY AC MEASUREMENT CYCLE
(Circuit Diagram DC400937 Sheet 2; Section 11 Page 11.6-3)

5.1.2.2 Wideband AC (WBV) Input

The WBV input measures AC voltages of between 1V and 3.5V over a frequency range of 10Hz to 20MHz, and voltages of between 100mV and 1V over a frequency range of 10Hz to 500kHz.

To achieve the 20MHz bandwidth required for the 3V range it employs a thermal voltage converter, coupled with an AC/AC transfer technique. By this means it compensates, at every reading, for time and temperature drift in the thermal converter's transfer characteristic.

For 100mV to 1V measurements over the 500kHz bandwidth, the 4920M switches the WBV input into the electronic RMS detector and uses the measurement technique described in section 5.1.2.1.

Measurements using the thermal voltage converter use an AC/AC transfer technique similar to that used for ACV input measurements. But for WBV inputs, a D-A converter is employed instead of the sample and hold circuit, allowing the 4920M's microprocessor to be included in the transfer loop.

The microprocessor is used to correct for linearity errors in the thermal converter's transfer characteristic. This is carried out before establishing the amplitude of the AC reference signal (generated during an AC/AC transfer) which accurately determines the thermal converter's transfer gain.

Four-Measurement Transfer
Each WBV measurement cycle requires the microprocessor to make four separate measurements using the instrument's A-D converter.

Measurement M1
During the first measurement (M1), the WBV input is applied to the thermal voltage converter, and the A-D converter measures the converter's DC thermocouple output – see Figure 5.1.2.2 (a). M1 is the value of the input signal multiplied by the AC/DC transfer gain of the thermal voltage converter.

$$M1 = G \times V_{WBV(RMS)} \quad \text{.....(1)}$$

Using the predetermined transfer characteristic of the thermal voltage converter (determined during a special calibration operation), the microprocesor calculates the RMS value of the WBV input (**M1'**) to an accuracy of around 1%. It then uses the instrument's 12-bit D-A converter and a precision voltage inverter to generate positive and negative DC voltages with an amplitude of M1'.

Measurements M21 and M22
After allowing the D-A converter to settle, the 4920M's A-D converter makes very accurate measurements of these positive and negative DC levels (**M21** and **M22** respectively) — see Figure 5.1.2.2 (b) and (c). A precision chopping circuit is then used to determine an AC reference signal (squarewave) of amplitude $\sqrt{\{ (M21^2 + M22^2) / 2 \}}$ called **DC_CHOP**.

Measurement M3
The fourth measurement (M3) is a measurement of the DC output of the thermal voltage converter's thermocouple with the AC reference signal (squarewave) applied to its input – see Figure 5.1.2.2.(d). The transfer gain of the thermal voltage converter at an input amplitude very close to the value of the WBV input is therefore given by the equation:

$$G = M3 / DC\_CHOP \quad \text{.....(2)}$$

Substituting equation (2) in equation (1) gives:

$$M1 = [\, M3 / DC\_CHOP \,] \times V_{WBV(RMS)}$$

and therefore:

$$V_{WBV(RMS)} = M1 \times DC\_CHOP \times M3$$

This equation is evaluated by the 4920M's microprocessor to determine the true RMS value of the WBV input signal from the four A-D measurements. In practice, to reduce noise and achieve highest possible accuracy, each of the four measurements is in itself the average of of four separate A-D conversions.

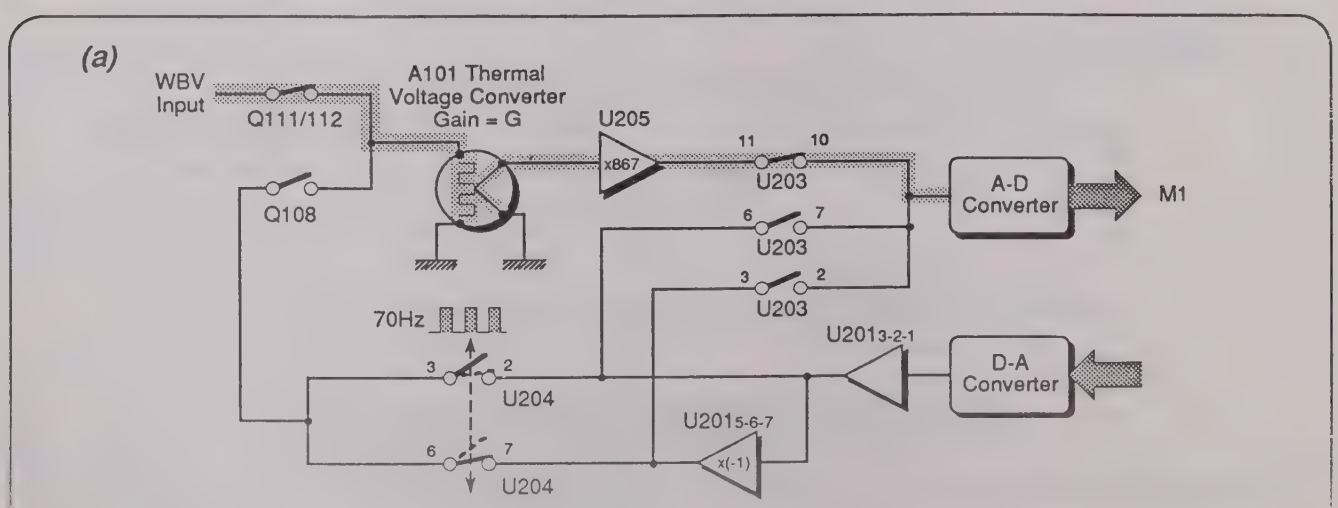


FIG.5.1.2.2 (a) WIDEBAND AC MEASUREMENT CYCLE
(Circuit Diagram DC400939 Sheets 1 & 2; Section 11 Pages 11.7-2/3)

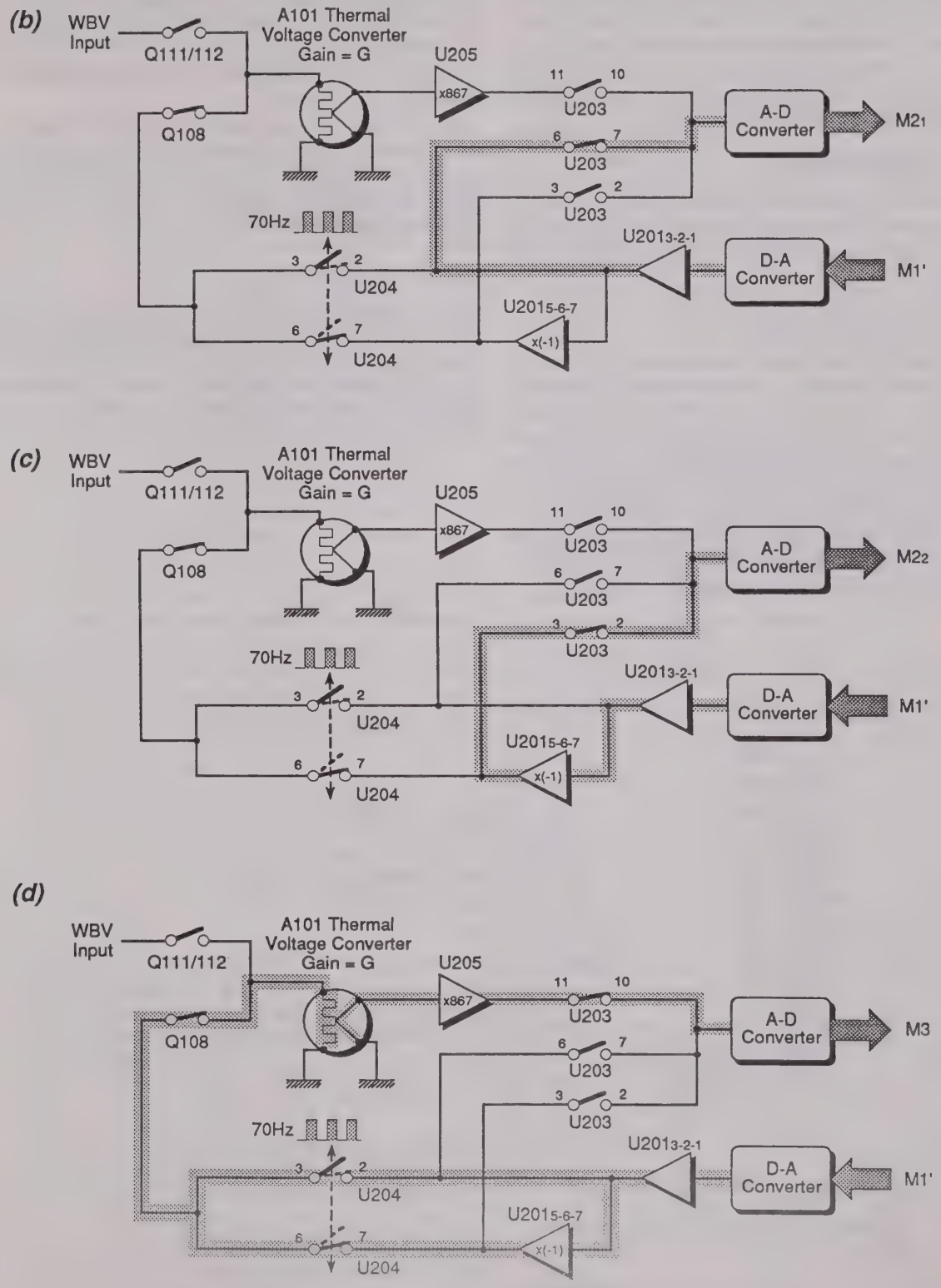


FIG.5.1.2.2 (b), (c), & (d) WIDEBAND AC MEASUREMENT CYCLE
(Circuit Diagram DC400939 Sheets 1 & 2; Section 11 Pages 11.7-2/3)

5.1.2.3 Analog to Digital Converter

The 4920M's multi-slope, multi-ramp A-D converter is a third-generation development of the basic dual-slope integrator and null detector converter. It has better than 0.2ppm linearity and high speed due to simultaneous application of the input signal voltage and reference voltage to the integrator. In addition, it uses a fixed 200msec conversion period to provide rejection of both 50Hz and 60Hz line supply generated noise.

5.1.2.4 Internal References

The reference voltages and currents for the A-D converter are derived from a specially conditioned and selected DC Reference Module which utilizes a temperature stabilized zener diode as its reference element.

5.1.2.5 Internal Serial Interface

The Internal Serial Interface is a data transfer system which allows the 4920M's analog circuitry, A-D converter and D-A converter to be controlled by passing control words through a single opto-isolator. It also provides a mechanism whereby the digital output of the A-D converter together with status bits from the analog circuits can be transferred back to the microprocessor via a single opto-isolator. Opto-isolation between the analog and digital control circuitry within the 4920M is necessary to prevent ground current noise being injected into the analog circuits, where it could otherwise affect the instrument's measurement accuracy.

On the analog side of the opto-isolation, the control word is clocked serially through a set of shift registers on the A-D and ACV converter PCBs until each bit is situated in the shift register location appropriate to its control function. At this time, the bits are clocked to the outputs of the registers where they control the instrument's analog state.

Some of the shift registers on the ACV and A-D converter PCBs are programmed to act as serial transmitters. The data bits presented at the inputs to these regisers are clocked into the serial stream, and returned through a single opto-isolator to the digital control sections of the 4920M.

5.1.2.6 Digital Circuitry

All control, keyboard, display and communication processing is performed by a MC68000 microprocessor. The 68000's firmware occupies 256kbytes of EPROM, while 64kbytes of RAM is provided for workspace, processor stacks etc. A further 8kbytes of battery-backed RAM provides non-volatile memory for the 4920M's autocal calibration constants.

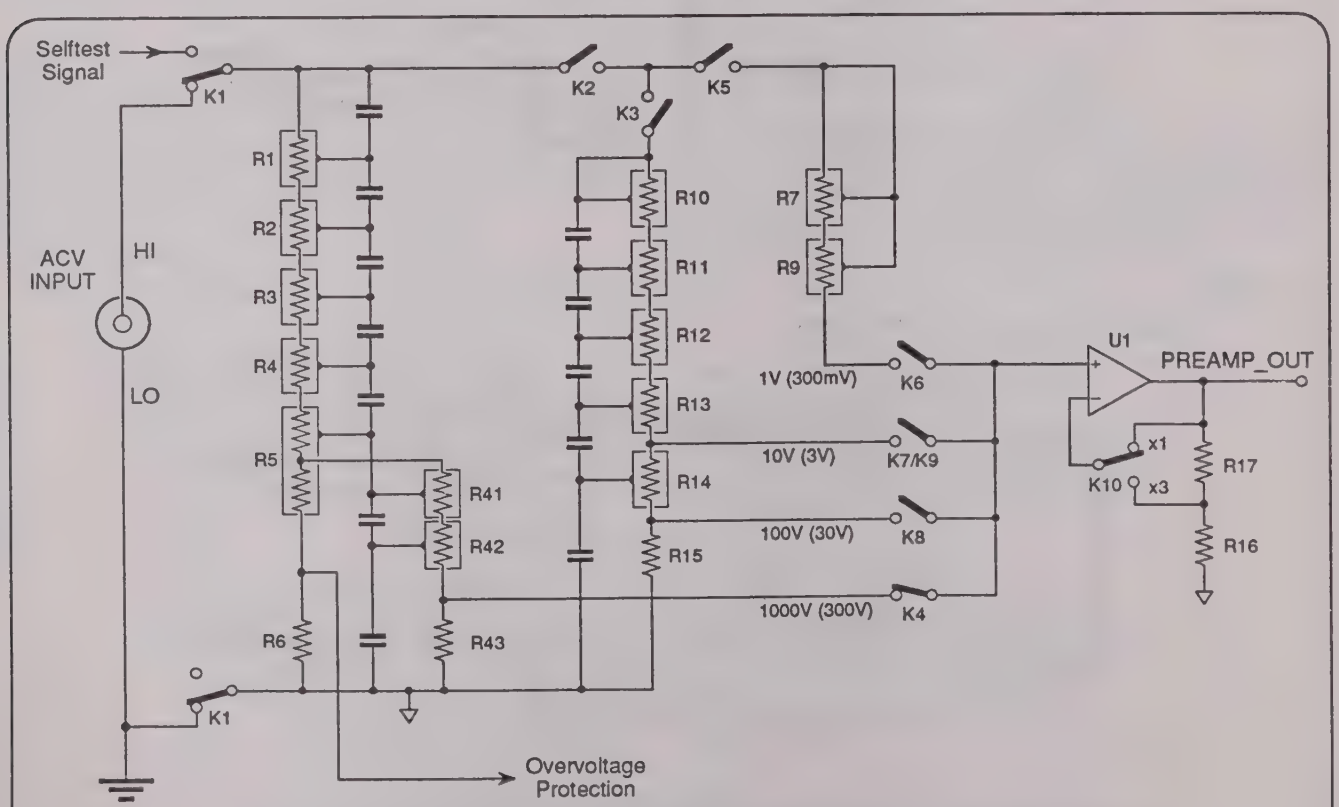


FIG.5.2.1.1 HIGH ACCURACY PRE-AMP PCB - SIMPLIFIED CIRCUIT DIAGRAM

5.2 PCB Descriptions

5.2.1 High Accuracy AC Pre-amp PCB

(Circuit Diagram DC400938 Sheet 1; Page 11.5-1)

5.2.1.1 Simplified Circuit Diagram

This is given as Fig. 5.2.1.1 on the page opposite.

5.2.1.2 Input Switching and Attenuators

The ACV input is switched to the High Accuracy AC pre-amp by relay K1 which isolates the ACV Hi terminal (center contact of the front-panel ACV coaxial connector) whenever the ACV function is deselected.
Note: When the ACV function is deselected, the ACV Lo terminal (outer contact of the ACV front-panel coaxial connector) remains connected to instrument ground.

When the ACV function is selected, K110-14/13-9/8-4 and K117-3 switch the ACV Hi and Lo terminals respectively to the ACV attenuator network. The ACV attenuator network is made up from hermetically sealed, high stability bulk metal foil resistors.

In order to maintain a flat frequency response for the attenuators it is necessary to eliminate the effect of stray capacitance between their internal resistance elements and their metallic encapsulations.

This is accomplished by making up each attenuator from a number of separate resistors (for example, R1 to R5 and R10 to R14), and driving their metallic encapsulations from a capacitive divider so that the instantaneous voltage on an individual resistor's encapsulation is approximately the same as the mean voltage on its resistance element. Because both ends of the stray capacitance experience approximately similar in-phase voltage excursions, the effect of the stray capacitance on the attenuator's frequency response is largely eliminated.

To obtain the required input ranges, the ACV attenuator network is switched as shown in Figure 5.2.1.1. The 10V and 100V attenuators produce a nominal 1V full range output and the 1000V attenuator produces a nominal 1.3V full range output, which is subsequently scaled when the microprocessor processes the output of the A-D converter.

The 4920M's 3V, 30V and 300V ranges use the 10V, 100V and 1000V attenuators respectively, producing respective nominal full range outputs of 0.3V, 0.3V and 0.43V. In the 1V and 300mV ranges, the ACV input is switched directly to the AC pre-amp via relays K1, K2, K5, and K6, and protection resistors R7 and R9.

5.2.1.3 Pre-amp Scaling

The AC pre-amp comprises operational amplifier U1 and feedback attenuator R16/R17. Relay K10 allows the pre-amp to be switched to unity gain for the 4920M's 1V, 10V, 100V and 1000V ranges, or to a gain of 3 for the instrument's 300mV, 3V, 30V and 300V ranges. U1 therefore produces an output of around 1V full range for all ranges up to the 100V range, and an output of 1.3V for the 300V and 1000V ranges.

5.2.1.4 Ground Current Compensation

Whenever the ACV function is selected, relay K101 on the High Accuracy AC PCB *(Circuit Diagram DC400937 Sheet 1; Page 11.6-2)* switches the output of the AC pre-amp to the input of U101 on the High Accuracy AC PCB. Operating as a unity gain inverting amplifier, U101 generates an output which is in anti-phase to that of the AC pre-amp.

This output is used to drive an anti-phase current into ground-4 (0V_4) (via 3KΩ resistor R105) which is equal in amplitude to the current injected by the AC pre-amp's 3kΩ gain defining network R16/R17. As a result , any AC errors due to current flow in ground-4 are eliminated.

5.2.1.5 Bootstrap Amplifier

To ensure a flat frequency response in U1, its effective input capacitance must be kept extremely low — to around 0.5pf or less. This is achieved by choosing an operational amplifier for U1 with low input capacitance and by providing it with positive and negative 'bootstrap' supplies which track its AC input signal. Because both ends of the op-amp's input capacitance therefore experience the same voltage excursions, the effective input capacitance of U1 is greatly reduced.

The bootstrap supplies are generated by the bootstrap amplifier built around Q1 to Q10. Q3, Q7, and Q4 form a very high speed, low input capacitance voltage follower which produces a low impedance bootstrap output (BS) that closely follows U1's input voltage. Zener diode D7 and emitter follower Q2 produce a low impedance positive bootstrap output (BS_HI) which tracks approximately 6.2V above BS, and zener diode D8 and Q10 produce a low impedance negative bootstrap output (BS_LO) which tracks approximately 6.2V below BS.

The collector-base junctions of Q11 and Q12 provide low-capacitance protection diodes which clamp U1's input to approximately +8V or -8V with respect to analog ground (via Q12/D8/D10 or Q11/D7/D9 respectively) during severe input overload conditions.

The BS supply is also used to reduce the effective stray capacitance in reed relays K4, K6, K8 and K9, and the effective input capacitance of matched dual J-FET Q3.

5.2.2 High Accuracy AC PCB

(Circuit Diagram DC400937 Sheets 1 to 6; Pages 11.6-1...7)

5.2.2.1 Simplified Circuit Diagram

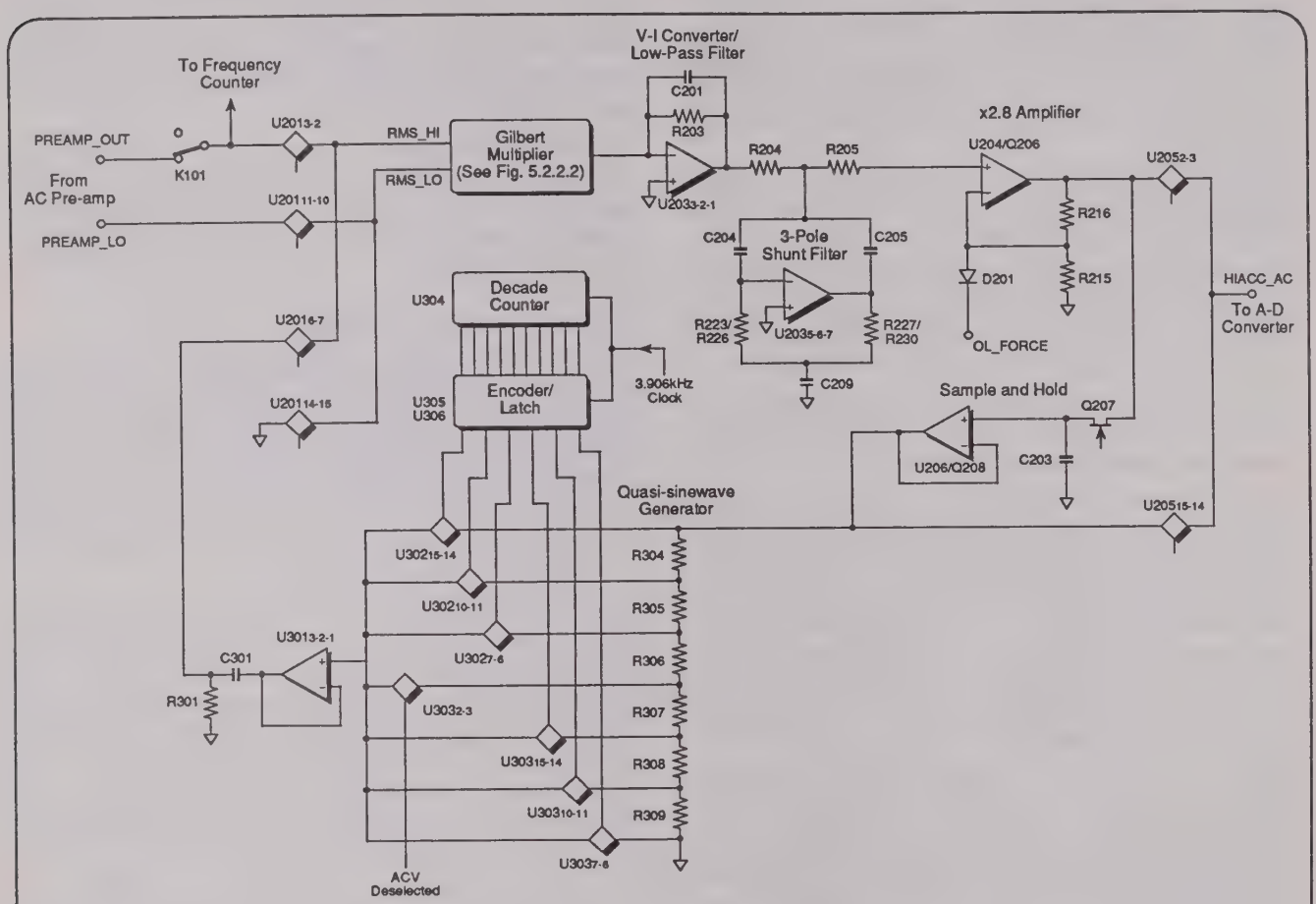


FIG.5.2.2.1 HIGH ACCURACY AC PCB - SIMPLIFIED CIRCUIT DIAGRAM

5.2.2.2 RMS Detector

The High Accuracy AC RMS detector is an electronic analog computer which computes the true RMS value of its input signal. The essential elements of the RMS detector are a Gilbert multiplier, a mean sensing filter, and a feedback loop which controls the multiplier's bias currents.

These elements are illustrated in Figure 5.2.2.1.

The output of the AC preamp is fed to both the X and Y inputs of the Gilbert multiplier so that it produces an output voltage which is given by the equation:

$$V_{out} = K_m \times V_{in}^2 / I_{bias}$$ where K_m is a constant ..... (A)

The filter then produces a DC output which is equal to the mean value of the multiplier output.
i.e.

$$V'out = \overline{Vout} = \frac{\overline{Km \times Vin^2}}{Ibias}$$

$$= Km \times \frac{\overline{Vin^2}}{Ibias} \quad \text{(since Ibias is a DC current)} \qquad (1)$$

The feedback loop then generates a multiplier bias current (Ibias) such that :

$$Ibias = Kf \times V'out \qquad (2)$$

Substituting equation (2) in equation (1) gives:

$$V'out^2 = K \times \overline{Vin^2} \qquad \text{where } K = Km / Kf$$

and hence

$$V'out = \sqrt{(K)} \times \sqrt{(\overline{Vin^2})} = K' \times \text{(the true RMS value of the input signal)}$$

K' is determined during each ACV measurement cycle by applying an AC reference voltage to the input of the RMS detector and measuring its output voltage. In addition, the amplitude of the AC reference is arranged to be very close to the output of the AC preamp so that the effect of linearity errors in the RMS detector is eliminated.

A simplified circuit diagram of the Gilbert multiplier is shown in Figure 5.2.2.2 (Overleaf).

5.2.2.2 RMS Detector (Contd.)

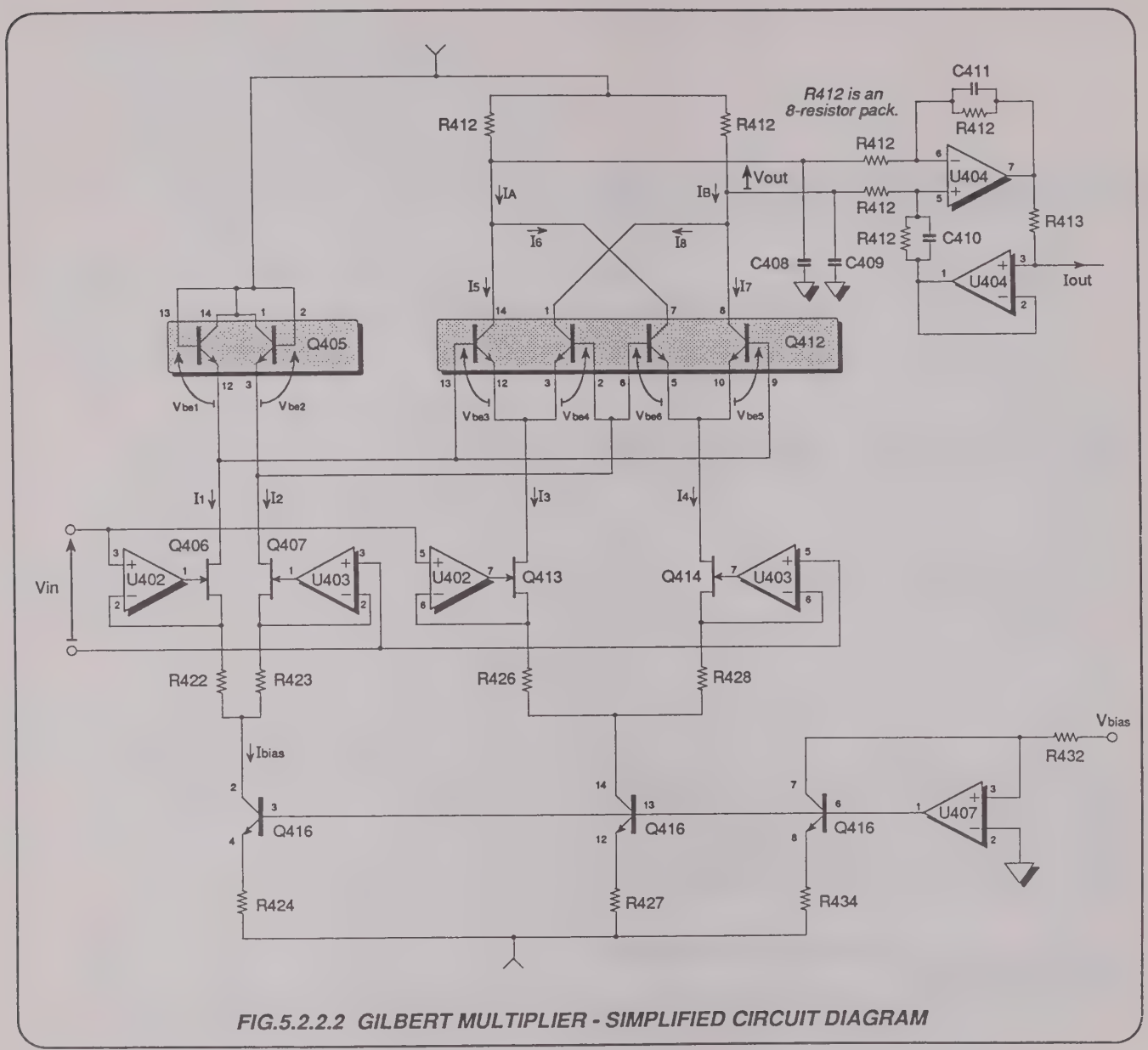


FIG.5.2.2.2 GILBERT MULTIPLIER - SIMPLIFIED CIRCUIT DIAGRAM

General Appreciation

The simplified circuit diagram of the Gilbert multiplier, shown in Figure 5.2.2.2, illustrates all the voltages and currents necessary to analyse the circuit's operation. A full analysis of this version of the circuit shows clearly that the differential output current, and the differential voltage Vout (developed across the two elements of R412 used as collector loads for Q412) are both proportional to the square of the input voltage.

The full analysis is omitted here, not only because of its length, but also because the calculations do not give an intuitive 'feel' to the way the circuit works.

The effects can be modelled as the mathematical action of multiplying numbers by adding their logarithms. Two separate routes are followed, each taking the logarithm of the input, then summing as they combine into the base-emitter voltages of the four transistors of Q412. Obtaining the result, by taking the antilog, corresponds to the action of the exponential transconductance of I_c/V_{be} in the same transistors.

The multiplier becomes a squarer because the two inputs to be multiplied are equal. The multiplying action of the circuit relies on the exponential transconductance between a transistor's base-emitter voltage and its emitter-collector current.

	I_c	is proportional to	$\exp(V_{be})$
so	V_{be}	is proportional to	$\mathrm{Ln}(I_c)$

Take the differential input voltage as **V.cosωt**. The difference between the currents I1 and I2 is linearly proportional to the differential input voltage (due to equal-value resistors R422 and R423).

$$I_1 - I_2 \propto V.\cos \omega t$$

The currents are drawn from the supply through Q405 (which is connected as two matched diodes) but because of their exponential transconductance, Q405 base-emitter voltages increase logarithmically with increase of emitter current. Therefore the differential voltage applied to Q412 bases, due to Q405 emitter currents, is logarithmic.

$$(V_{Q405\text{-}3} - V_{Q405\text{-}12}) \propto Ln(V.\cos \omega t)$$

The difference between the currents I3 and I4 is also linearly proportional to V.cosωt (again due to equal-value resistors R426 and R428). But now each current is divided between the emitters of the two transistors used as drain load. The cross-connections of their collectors ensure that a differential balance is maintained: each of the four collector currents responds to its individual transistor's total V_{be}, while I3 and I4 remain linear.

There are now two effects operating on each of the transistors of Q412 in summation: the logarithmic voltage applied to the base, and the linear emitter current which also introduces a logarithmic base-emitter voltage.

Because of the exponential transconductance and the differential balance, each individual transistor's collector current will be the result of taking the antilogarithm of the two summated log voltages (i.e. is proportional to the product of the two original voltages).

By cross-coupling the collectors of Q412, other constant terms are suppressed. The net current in one R412 collector load resistor varies in proportion to:

$$\exp[2 \times Ln(V.\cos\omega t)] = \exp[Ln(V.\cos\omega t)^2] = (V.\cos\omega t)^2$$

and in the other:

$$-\exp[2 \times Ln(V.\cos\omega t)] = -\exp[Ln(V.\cos\omega t)^2] = -(V.\cos\omega t)^2$$

As a result, the differential voltage **Vout** is also proportional to $(V.\cos wt)^2$, and the circuit has performed an analog squaring of the input voltage, together with a linear scaling. This scaling effect is controlled by the gain of the external circuit, coupled with bias feedback. The whole transfer function is given by the equation (A) of para 5.2.2.2 (page 5-8):

$$V_{out} = K_m \times V_{in}^2 / I_{bias}$$

Variation of the differential temperatures in the base/emitter junctions of the log/antilog transistors has an effect on the gain factor K_m. This variation is minimized by the use of matched transistors in the same thermal environment (Q405 and Q412).

Circuit Detail

Referring to *Circuit Diagram DC400937 sheet 4, page 11.6-5*, transistors Q4055-6-7 and Q40510-9-8 are included to buffer the signals applied to the transistors in Q412 from the capacitance at the emitters of transistor pair Q40512-13-14/Q4053-2-1, and cascode transistors Q4103-2-1/Q4105-6-7 and Q41615-16-1/Q41611-10-9/Q417 are required to achieve the very high output impedance required in the output and bias current sources respectively. Transistors Q401/Q402 and Q403/Q404, together with zener diodes D401 and D402, provide bootstrap supplies for U402 and U403 so that these amplifiers reject the common mode voltages which appear at their inputs.

As explained earlier in this section, feedback is applied via the BIAS signal in order to make the circuit RMS sensing.

Because U407 and Q4168-6-7 maintain U4073 as a virtual ground point, a current defined by V_{BIAS}/R_{432} flows in the collector of Q4168-6-7. The same current flows in current mirrors Q4164-3-2 and Q41612-13-14 (which thermally track and are matched to Q4168-6-7 by virtue of being monolithically integrated into the same package) to provide appropriate bias curents the multiplier.

U4045-6-7 and U4043-2-1 convert the differential voltage developed across the Gilbert multiplier's load resistors into a single ended current which flows in the output RMS_OUT. The transconductance gain of this circuit is given by $-1/R_{413}$.

U2033-2-1 then converts the RMS_OUT current into a single ended voltage in order to drive the mean sensing filter built around U2035-6-7. This filter is 3-pole shunt filter which introduces no DC error into the signal path between U2031 and U2043.

The overall transfer gain between the inputs to the RMS detector and U2043 is arranged to be approximately unity — i.e. a given RMS signal amplitude at the input to the RMS detector produces approximately the same value DC voltage at U2043.

Op-amp U2043-2-6 then amplifies this DC voltage by a factor of 2.8, as defined by resistors R215 and R216. This gain is necessary because during the second and third A-D conversions in an ACV input measurement cycle the output voltage of U2043-2-6 is held on capacitor C203 where it defines the peak-to-peak amplitude of the quasi-sinewave that is used in the accurate determination of the RMS detector gain.

U2043-2-6 must therefore multiply the DC signal at its input by the ratio between the peak-to-peak and RMS values of a sinewave; i.e: 2 x 1.414 : 1, or approximately 2.8 to 1. (The quasi-sinewave is deliberately synthesized so that its RMS: peak ratio is the same as that for a sinewave.) By accurately determining the RMS detector gain using a quasi-sinewave of approximately the same RMS amplitude as the input signal, the effects of linearity errors in the RMS detector are eliminated.

5.2.2.3 Sample-Hold and Quasi-Sine Generator

During the first of the three A-D conversions required to accomplish an ACV input measurement (see section 5.1.2.1), CMOS switch U2013-2/11-10 applies the output of the AC pre-amp to the input of the RMS detector, and U2052-3 applies the output of the RMS detector to the A-D converter. During this period J-FET Q207 is on, allowing C203 to sample the output voltage of the RMS detector.

At the end of this first conversion, Q207 turns off so that the RMS detector output voltage is held on C203. U206/Q208 buffer the voltage on C203 to provide a low impedance voltage source which defines the amplitude of the AC reference signal during the second and third A-D conversions in the ACV measurement cycle.

During the second measurement cycle, U20515-14 routes the sample/hold output voltage to the A-D converter so that it can be accuractely measured. This measurement eliminates any DC errors in the sample/hold circuit when determining the gain (K') of the RMS detector.

The output of the sample/hold circuit drives the input to the quasi-sinewave generator. The resisitive divider R304 to R309 produces voltage levels which are 8.461%, 34.930%, 65.070% and 91.538% of V_O. Together with V_O and analog ground, these voltages provide all the levels required to generate the quasi-sinewave shown in Figure 5.2.2.3.

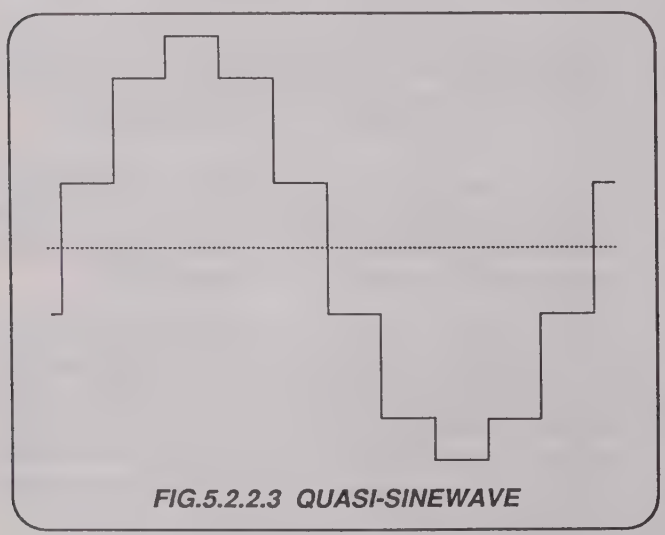


FIG.5.2.2.3 QUASI-SINEWAVE

CMOS switches U30215-14/10-11/7-6 and U30315-14/10-11/7-6, controlled by decade counter U304, select the voltage levels in the appropriate order so that the quasi-sinewave is synthesized at the input to buffer amplifier U3013-2-1. OR-gate U305 encodes the output of the decade divider because each output level from resistive divider R304 to R309 is required twice in each cycle of the quasi-sinewave, and hex latch U306, which is clocked on the opposite clock edge to decade counter U304, de-glitches the U304/U305 outputs.

The decade counter is clocked by clock signal QS_CLK at 3.906kHz, giving the output of the quasi-sinewave generator a fundamental frequency of 390.6Hz.

The voltage levels used to synthesize the quasi-sinewave are chosen such that higher order components (for example, $\sin^3$ or $\sin^4$ components), which are generated due to imperfections in the RMS detector's square law, have the same amplitude for both the quasi-sinewave and the ACV sinewave input. The positive DC offset in the quasi-sinewave (0.5 x V_O) is removed by C301/R301 to produce an output from the quasi-sinewave generator (QS_HI) which is symmetrical with respect to analog ground.

During the first A-D conversion of the ACV measurement cycle (when the output of the AC pre-amp is applied to the RMS detector) or when the ACV function is deselected, the quasi-sinewave generator is disabled via signals A_H and A_L. During this period, A_H holds the decade counter U304 in its reset condition via its CT=0 input, and A_L holds all of U306's latches in reset via U306's R input, forcing all the CMOS switches which are used to generate the quasi-sinewave into the off condition. At the same time, A_H switches CMOS switch U3032-3 on so that capacitor C301 charges to 50% of V_O via unity gain buffer U3013-2-1. This ensures a clean start to the quasi-sinewave when the quasi-sinewave generator is re-enabled.

U3015-6-7 is used to inject DC and AC currents into ground-6 (0V_6) which are of equal amplitude but opposite polarity/phase to those flowing in resistive divider R304 to R309, and resistor R301. This eliminates ground current noise in ground-6 due to these currents.

5.2.2.4 Overload Detection

Analog detection of input overloads is performed by tap R6 at the bottom end of the 1000V/300V input attenuator on the AC Preamp PCB *(Circuit Diagram DC400938 Sheet 1; Page 11.5-1)*. R6 develops a voltage of approximately 1.9V RMS for an ACV input overload of 1100V RMS. This signal (OL_SIG) is fed to op-amp U1025-6-7 on the High Accuracy AC PCB which is configured as a precision rectifier. The rectified signal appearing at the junction of R108/R111 is filtered by the mean sensing active filter based around U1023-2-1 to produce a DC overload signal OL_LEV.

Transitions from normal to overload conditions are detected by feeding the OL_LEV signal to the Schmitt trigger threshold detector based around op-amp U6059-10-7. The output of this detector (OL_L) is low during overload conditions and is used to force various conditions in the 4920M's High Accuracy AC analog circuitry. It is level shifted by U5043-2-1 and used to force an overload condition (via diode D201) at the output of the RMS detector in order to force the A-D converter into an overload condition. Via NAND-gates U5031-2-3 and U5034-5-6 and level shifters U5055-6-7 and U50510-9-8 it also forces the atenuator switching relays on the AC Pre-amp PCB into the 1000V range condition.

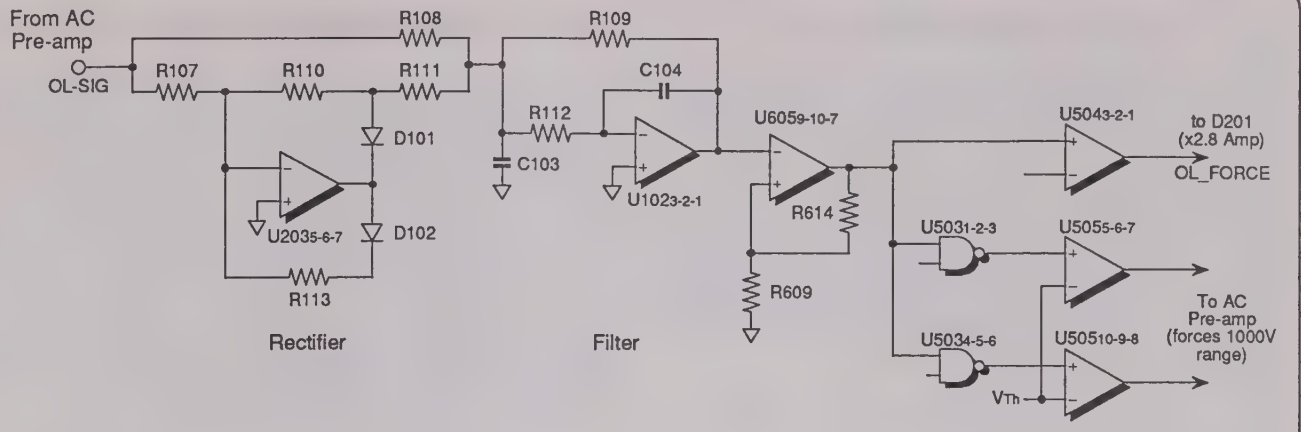


FIG.5.2.2.4 OVERLOAD DETECTION

5.2.2.5 Frequency Detection

The output of the AC pre-amp (or the output of the WBV 1V range buffer in WBV mode) is fed to the input of high-gain differential amplifier Q101/Q102 via C105. Schmitt trigger U6054-5-12 detects the zero crossings of the AC output from this differential amplifier, providing a squarewave input for the FSIG input of frequency counter IC U606. U606 is gated by the output of timer U603 which is triggered each time an A-D conversion is initiated. U603 can produce gate periods of 32 msec if Q603 is off, or 700 msec if Q603 is on. Q603 is turned on and off by the 4920M's microprocessor via a control bit in the timer counter IC which drives the GCNTR output. In the 4920M, the 700msec gate period is permanently selected.

The precise gate period is not critical because the counter IC U606 contains two separate counters — one of which counts FSIG cycles while the other counts cycles of the 4MHz reference clock (FREF), generated by crystal oscillator Y601. At the end of the gate period the counter IC automatically divides the number of FREF cycles by the number of FSIG cycles and makes the result available for transmission to the 4920M's microprocessor via the internal serial interface bus. Because FREF is known to be 4MHz, the microprocessor can calculate FSIG from the division ratio.

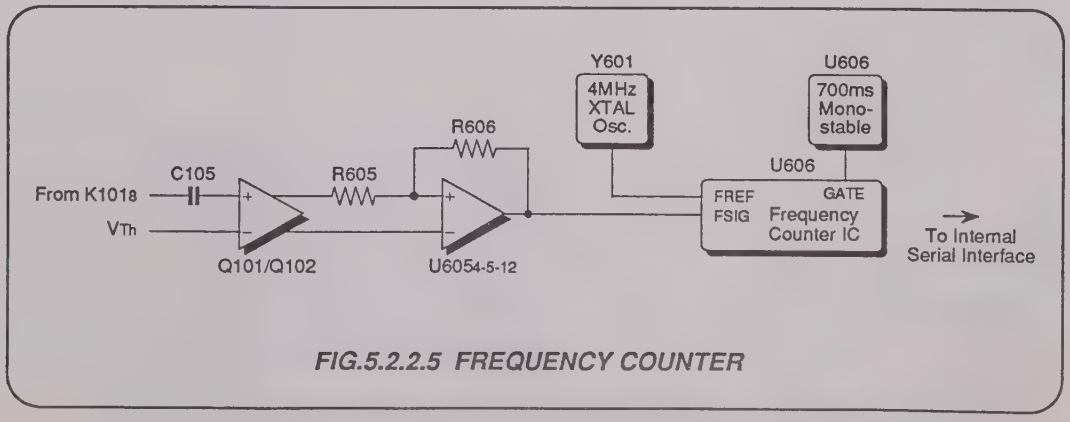


FIG.5.2.2.5 FREQUENCY COUNTER

5.2.3 Wide Band AC PCB

(Circuit Diagram DC400939 Sheet 1 and 2; Pages 11.7-2/3)

5.2.3.1 Simplified Circuit Diagram

The WBV measurement function's thermal voltage converter is only used to provide the WBV 3V range which requires an input bandwidth from 10Hz to 20MHz. The WBV 1V range, which only requires a bandwidth of 10Hz to 500kHz, uses the same electronic RMS detector that is used for ACV input measurements.

Therefore, when the WBV 1V range is selected, K1014-3 and K1017-8 route the WBV input to unity gain inverting amplifier U1013-2-1 on the High Accuracy AC PCB assembly via K1014-3 on the High Accuracy AC PCB assembly *(Circuit Diagram DC400937 Sheet 1; Page 11.6-2)*.

The output of this inverting amplifier is fed via K1017-8 on the High Accuracy AC PCB assembly to the input of the 4920M's electronic RMS detector.

Note: When the WBV function is deselected, the WBV Hi terminal (center contact of the front-panel WBV coaxial connector) remains connected to the 4920M's internal 50Ω load, and the WBV Lo terminal (outer contact of the front-panel WBV coaxial connector) remains connected to instrument ground.

5.2.3.2 Thermal Voltage Converter

The WBV input connects to resistor array R105 to R111 which together with R103, R104, factory selected value R135, the resistance of the thermal voltage converter, and the 'on' resistance of J-FETs Q111 and Q112 make up a precision 50Ω load.

For the first of the four A-D conversions required to make a WBV 3V range measurement, the ACHF-L signal turns Q113 off via CMOS switch U20411-10, allowing J-FETs Q111 and Q112 to turn on, connecting the thermal voltage converter to the input signal. The output from the thermal voltage converter's thermocouple (around 7mV full range) is amplified by U205 to provide a full range output voltage of approximately 6V.

U20311-10 routes this signal to the 4920M's A-D converter so that the microprocessor can make an initial estimate of the WBV input voltage using the predetermined transfer function of the thermal voltage converter (determined during 'special calibration').

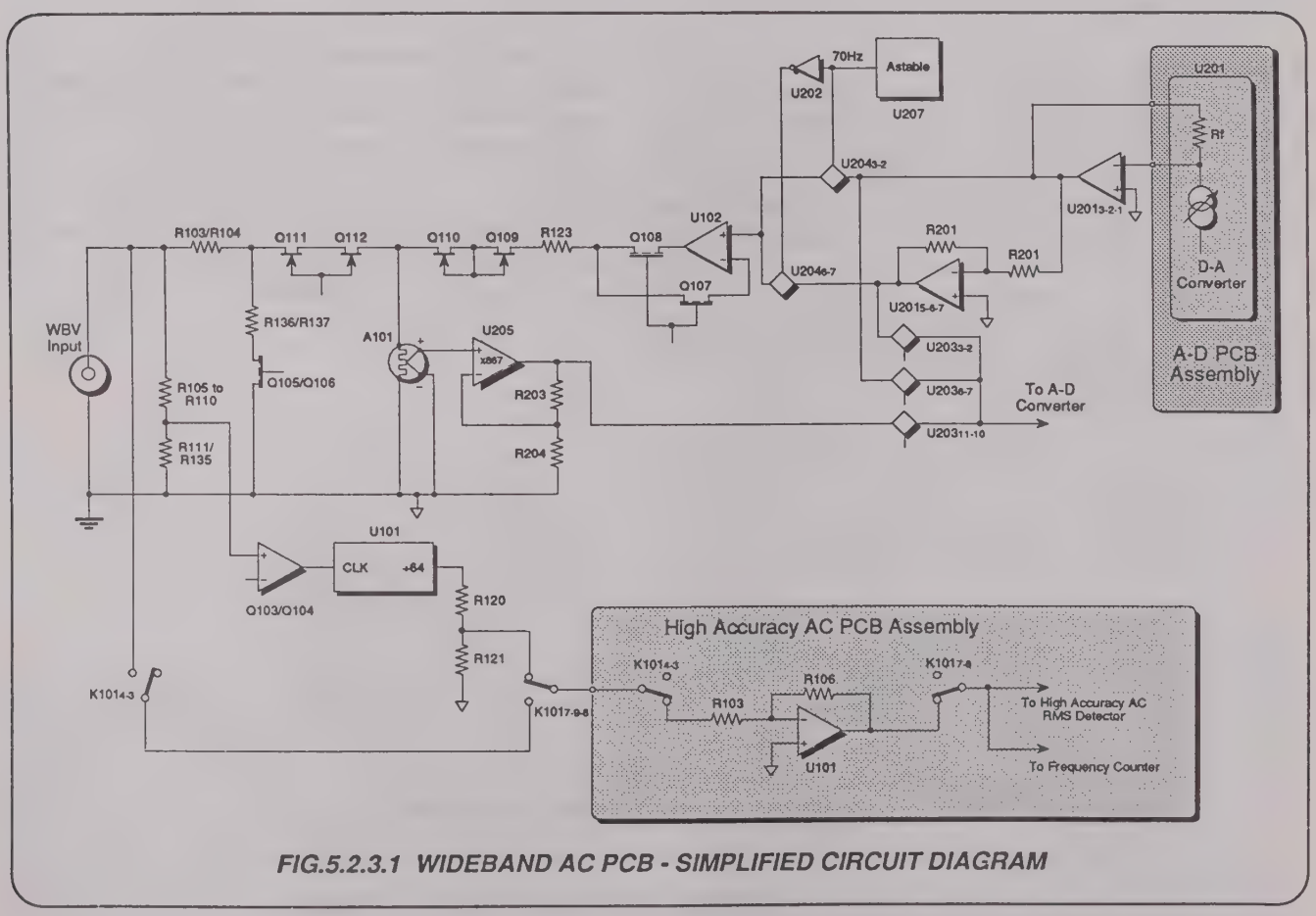


FIG.5.2.3.1 WIDEBAND AC PCB - SIMPLIFIED CIRCUIT DIAGRAM

5.2.3.3 Digital to Analog Converter

Based on this initial estimate of the WBV input value (accurate to around 1%), the microprocessor generates a DC voltage of the same RMS value as the estimate by transferring a digital input to 12-bit multiplying D-A converter U201 on the A-D PCB assembly *(Circuit Diagram DC400936 Sheet 2; Page 11.4-2)*. The voltage reference for the D-A converter is produced by zener diodes D202 to D204 which produce a reference voltage of 3.66V.

The current output from the D-A converter is converted to a voltage by U2013-2-1 and this voltage is then inverted by voltage inverter U2015-6-7. U2013-2-1 and U2015-6-7 therefore produce highly stable positive and negative DC voltages respectively, close to that of the RMS value of the WBV input signal.

5.2.3.4 DC Chopper

As part of the second and third A-D conversions of a complete WBV measurement cycle, CMOS switches U2043-2 and U2046-7 are turned on during alternate half-cycles of the 70Hz squarewave generated by astable multivibrator U207. Thus a 70Hz squarewave signal is produced (DC_CHOP), which has an RMS value equal to $\sqrt{\{ (M21^2 + M22^2) / 2 \}}$, where M21 and M22 are the two opposite-polarity results of measurement M2. The DC_CHOP signal is buffered by voltage follower U1023-2-6.

During the second, third and fourth conversions of a WBV measurement cycle the buffered signal is applied to the thermal voltage converter by turning Q108 on (during the second and third conversions for settling only). At the same time Q111 and Q112 are turned off so that the WBV input is disconnected from the thermal voltage converter, and Q105 and Q106 are turned on, replacing the thermal voltage converter by R137 in parallel with factory selected value R136, so that the input impedance at the WBV input remains unchanged at 50Ω.

Q107 is included so that the on resistance of Q108 is in the feedback loop of U102 and therefore does not attenuate the buffered DC_CHOP signal. It also isolates U102 from the WBV input while the WBV input is applied to the thermal voltage converter. J-FETS Q109 and Q110 (which have on resistances matched to Q111 and Q112 respectively) and R123 (which is equal in value to R103 + R104) are included so that the buffered DC_CHOP signal sees exactly the same thermal voltage converter load that is experienced by the WBV input signal.

5.2.3.5 Frequency Pre-scaler

Because the WBV 3V range will accept input frequencies as high as 20MHz, frequency pre-scaling is required before the input frequency can be measured.

Q103/Q104 are connected to form a high-gain high-speed amplifier which squares up the signal derived from voltage divider R105/R111/R135. The output from this amplifier drives the clock input (pin 11) of ripple counter U101, while R116 provides sufficient hysteresis at this input to prevent false clocking of the counter.

5.2.4 Analog-to-Digital Conversion

5.2.4.1 Functional Diagram

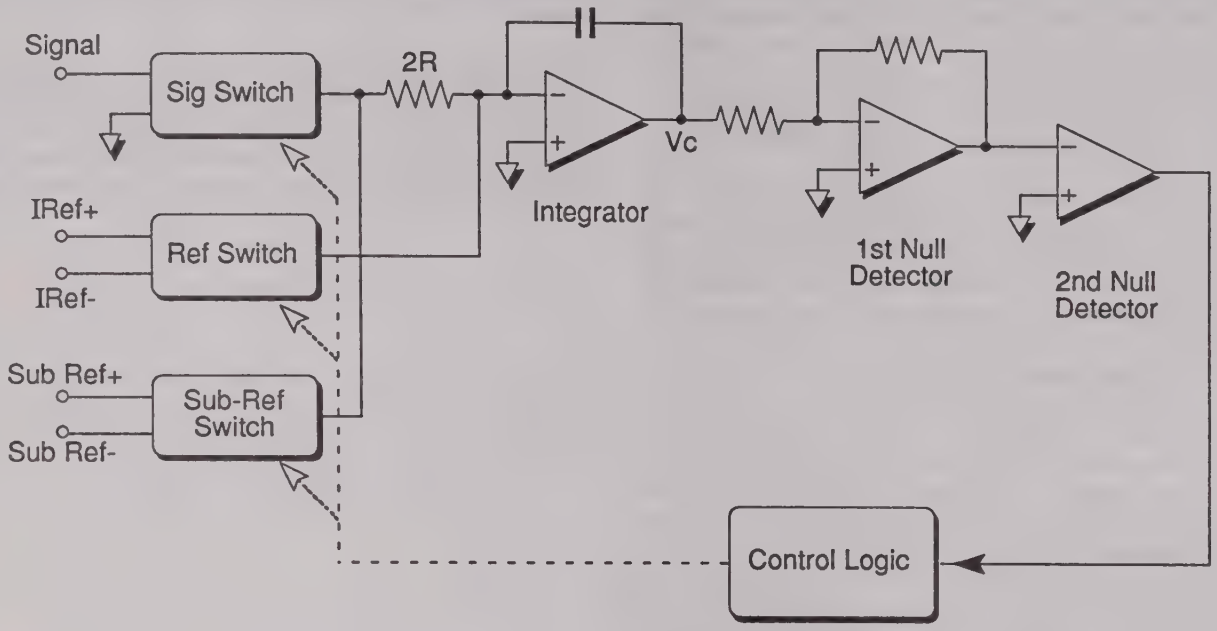


FIG. 5.2.4.1 A-D CONVERTER - SIMPLIFIED SCHEMATIC

5.2.4.2 Introduction

The instrument converts conditioned analog signals to a digital form using a multi-ramp, multi-slope, integrating A-D. This provides:

High linearity - < 0.2ppm without adjustment
Low Noise - < 0.05ppm of full scale
High Speed - signal and reference are applied simultaneously, greatly reducing the conversion time

A digital autozero system avoids the need for the more common sample-and-hold type of autozero circuit.

Multislope operation permits the integration capacitor value to be smaller than normally required for a more conventional circuit, greatly reducing problems due to dielectric absorption.

The control logic determines the parameters of the conversion, by counts and timings which are selected by the 4920M's microprocessor and transferred via the internal serial interface in four bytes of data. Timing, counting and control are executed by a custom A-D converter control ASIC (Application-Specific Integrated Circuit).

The digital result of a measurement is transferred back to the processor via the internal serial data interface.

Reference switching errors are reduced to constant values, the sum of which is subtracted from the reading by the microprocessor.

Note:

Pages 5-17 to 5-20 contain illustrations of the A-D conversion cycles used in the 4920M. Because of the wide range of signal amplitudes involved, the waveforms given in the figures are not to scale - some exaggeration being required to show the changes. The control signal waveforms are intended to illustrate sequencing only - polarities and amplitudes in the figures are therefore not to be regarded as accurate.

5.2.4.3 Reset

'Reset' mode replaces the more conventional analog 'Autozero'. It is imposed by the A-D converter control ASIC except when a conversion is in progress. The four phases of reset activate the converter to ramp through small excursions about zero, eliminating zero drift and holding the converter in a quiescent state. The ramps and timings are shown in Fig. 5.2.4.2.

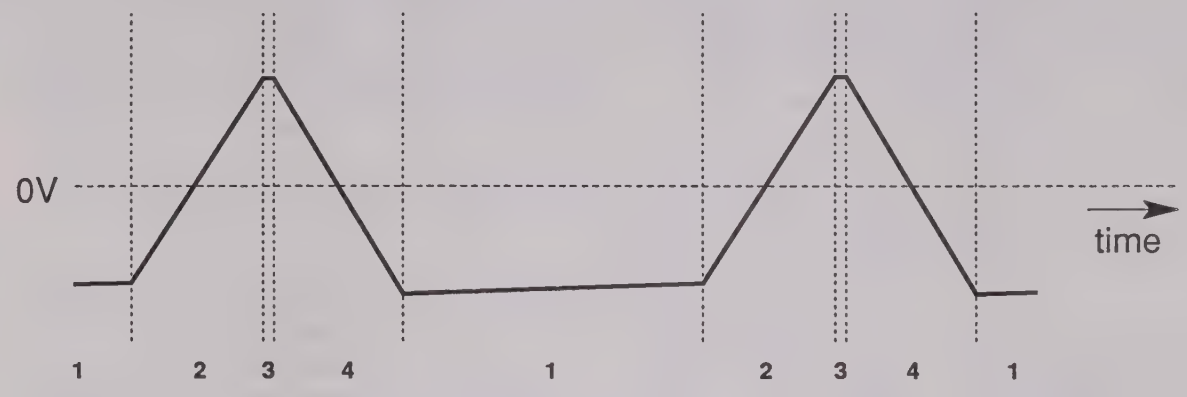


FIG. 5.2.4.2 A-D CONVERTER - RESET CYCLE

The Reset Cycle

There are four phases in the reset cycle, as illustrated in Fig. 5.2.4.2:

ø1. Zero is applied to both Signal and Reference inputs. This time is set by the A-D converter control ASIC, and the slope is determined by the integrator drift (shown much exaggerated in the diagram).

ø2. Zero is applied to the Signal input, and -Ref/256 to the Reference input. The integrator ramps up and crosses zero. The Null Detector has a fixed delay, and for a further fixed period after this, the A-D converter control ASIC continues to apply -Ref/256. These three times constitute the time of phase 2.

ø3. Zero is applied to both Sig and Ref inputs as in phase 1 for a very short period, to guard against any overlap in switching. The integrator drifts during this time.

ø4. Zero is applied to the Signal input, and +Ref/256 to the Reference input. The integrator ramps down and crosses zero. The Null Detector has the same delay, and again the A-D converter control ASIC continues to apply the +Ref/256 for a further fixed period. These three times constitute the time of phase 4.

The cycle is repeated, maintaining the integrator output near zero (within approx. 25µV). The overshoot in phases 2 and 4 is deliberately introduced to ensure a clean transition through zero. As can be seen from the diagram, the integrator output always reaches the same value at the end of Phase 4, due to the two fixed ramps, even though drift may occur in phase 1.

Because of its low amplitude and short timings, this reset waveform is difficult to view accurately.

End of Reset

The A-D continues in Reset mode until instructed to start a reading conversion. A separate control line (CI1-R), with its own opto-coupler (U6033-6), initiates the conversion.

5.2.4.4 Conversion Initiation

Triggering

The 4920M can start a measurement cycle as a result of an external trigger, a manual trigger (front-panel SAMPLE keyswitch) sample, a trigger received over the IEEE 488 interface, or a trigger generated by the instrumenet's own internal free-running trigger source. The number of A-D conversion cycles required in a measurement cycle depends on the function selected - for example, the ACV or WBV function .

'Conversion Initiate' Signal

For each A-D conversion required, the **Conversion Initiate** signal (CI1-R) is set high to start a conversion on its rising edge. As a result, the A-D executes a Reset cycle, ensuring that the conversion starts from a known integrator output value. The cycle is terminated by the A-D converter control ASIC SIG lines being activated to apply the conditioned signal to the integrator input. The result of CI1-R is shown in Fig. 5.2.4.3 for a negative signal input.

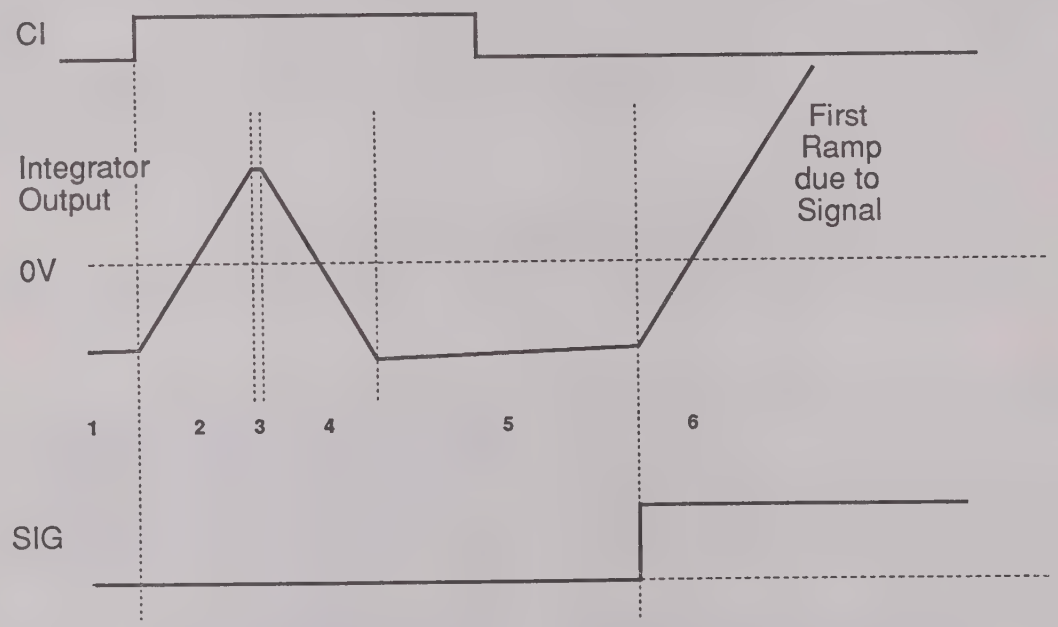


FIG. 5.2.4.3 A-D CONVERTER - EFFECT OF 'CONVERSION INITIATE' SIGNAL

5.2.4.5 Multiple-Ramp Conversion

Sequence of Phases

The integrator output and control signals for the 200msec period, multiple-ramp conversion utilized in the 4920M are illustrated in Fig. 5.2.4.4.

ø1 to ø5 These are the Reset phases described in sections 5.2.4.3 and 5.2.4.4.

ø6. The conditioned input signal (always positive) is applied to the Sig input, with zero on the Ref input. The integrator ramps down for a fixed period.

ø7. The input signal is applied to the Sig input, with +Ref on the Ref input. This 'bias' is applied for a fixed period causing the integrator to ramp further away from null.

ø8 and ø9: Zero is applied to both Sig and Ref inputs to ensure that two references are not applied together.

ø10. Zero is applied to Sig input and -Ref to the Ref input. The integrator ramps up and eventually crosses the null detector threshold. The Null Detector has a standard fixed delay, during which the A-D converter control ASIC continues to apply -Ref. The integrator therefore overshoots.

ø11. Zero is applied to Sig and Ref inputs for a fixed period. Note that the conditions of phase 11 are applied three times.

ø12. Zero is applied to the Sig input and +Ref/16 to the Ref input. The integrator ramps down and crosses the null point. The Null Detector again has a fixed delay and the A-D converter control ASIC therefore continues to apply the +Ref/16 for a further fixed period, causing the integrator to overshoot.

ø13. Zero is applied to Sig input and -Ref/16 to the Ref input. The integrator ramps up and overshoots the null, once again determined by the Null Detector and ASIC delays.

ø14. Zero is applied to Sig input and +Ref/256 to the Ref input. The integrator ramps down very slowly and crosses the null. The integrator overshoots null, once again controlled by the Null Detector and ASIC delays.

ø15 The positive input signal is reapplied to the Sig Input .

ø16 Sig and Ref are applied. The polarity of the chosen reference is such as to ramp back towards null. The ramp overshoots null due to null detector and ASIC delays.

ø17 Sig only is applied. No 'wait' time is required between ø16 and ø17, as the reference is not applied in ø17, and so there is no possibility of shorting two references together. The slope of the ramp is the same as in ø6.

The cycle of phases 17, 7, 15 and 16 continues 128 times, each cycle taking 1.568ms to complete. The total conversion time is therefore 200msec.

Once again, the accumulated amount of the references applied is a measure of the input signal.

Integrator Output Waveshape

As the magnitude of the input changes, so does the shape of the integrator waveform.

At full scale the ramps are symmetrical and of equal height. As the signal is reduced, the ramps begin to lean over with the null point moving to the left. The first ramp is reduced to about half the size of subsequent ones, and they are not all the same size. This is normal behavior, and is not indicative of a fault.

Counting

The rules for counting the amount of reference applied are quite simple:

1. Counting occurs whenever a reference is applied.
2. The count is **up** for negative references; **down** for positive references.
3. If Ref is applied the count increments in units of 256.
4. If Ref/16 is applied the count increments in units of 16.
5. If Ref/256 is applied the count increments in units of 1.

This ensures that even with overshoot the correct result is obtained. A normal 32-bit up/down counter within the A-D

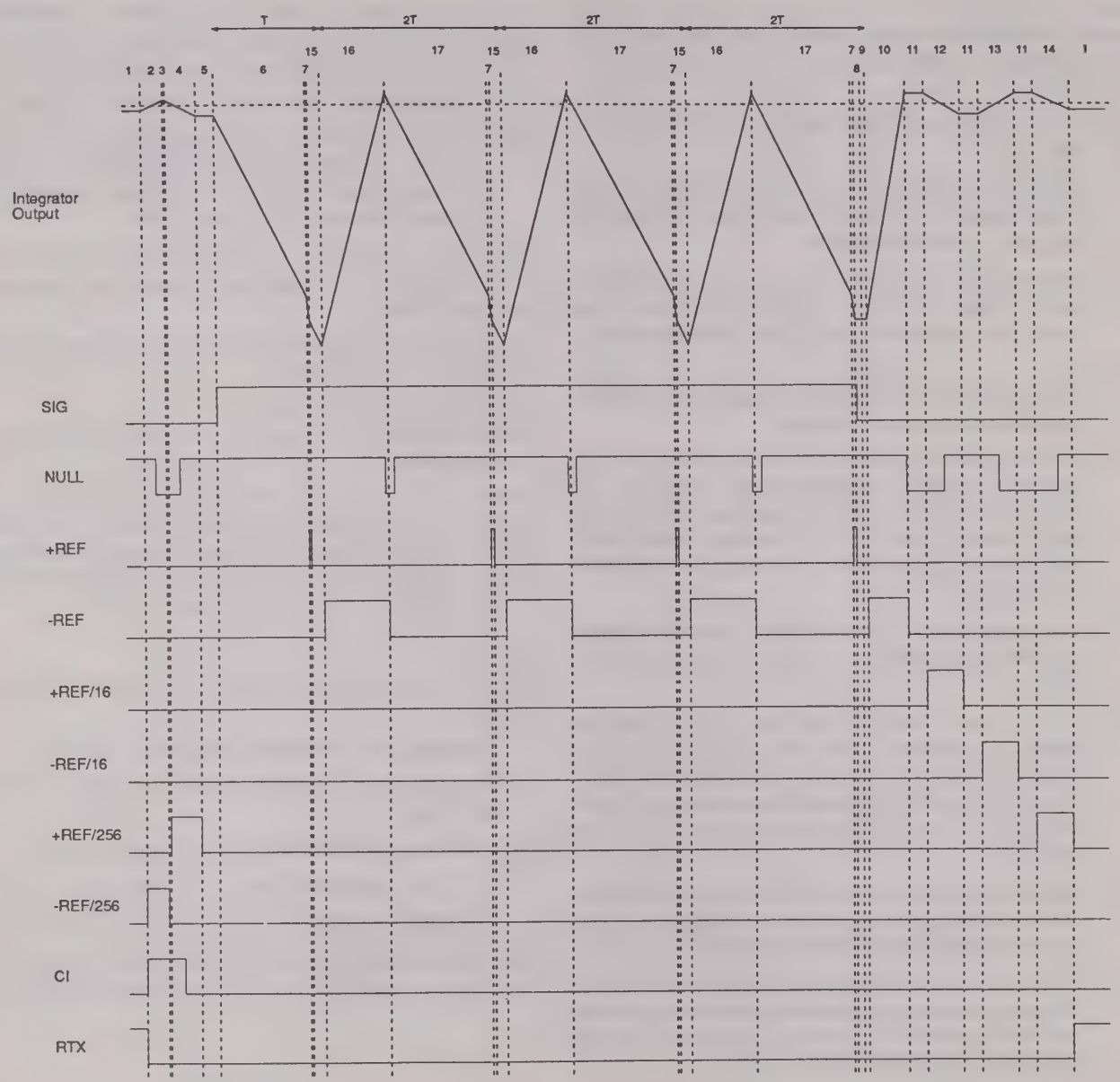


FIG. 5.2.4.4 MULTIPLE RAMP CONVERSION - POSITIVE INPUT

5.2.5 Internal References

(Circuit Diagram DC400936 Sheet 4; Page 11.4-4)

5.2.5.1 Master Reference

Module Description

The master reference used in the 4920M's A-D converter is derived from a specially conditioned voltage reference module, which contains a precision zener reference diode together with temperature control circuitry. By maintaining the zener diode and its associated components at a constant temperature, reference voltage drift caused by the zener diode's temperature coefficient.is largely eliminated.

The reference module produces an output voltage which is stable to within ±3ppm per year, produces output noise of less than 0.1ppm, and has a temperature coefficient of less than 0.1ppm/°C. This temperature coefficient is held over a very wide temperature span of 0°C to 70°C, and the references exhibit negligible temperature shock hysteresis.

Master Reference Generation

The HI and LO outputs of the 7.23V reference module (REF1) feed op-amps U4045-6-7 and U4043-2-1 respectively. Together with Q402 and Q403 these op-amps impress voltage REF1 across resistor network R4169-8/6-11/13-4/2-15 which make up a 15kΩ resistor. A current of 0.482 mA therefore flows in this 15kΩ resistor and in the source and drain of Q402 and Q403. Op-amps U4073-2-1 and U4075-6-7 operate as active current mirrors so that a current of the same value flows out of IREF_POS and in to IREF_NEG.

REF1 is also buffered, inverted, and attenuated by a factor of 4 in op-amp U4063-2-1 to produce VREF2_NEG, which is then inverted by unity gain inverting amplifier U4065-6-7 to produce VREF2_POS. VREF2_NEG and VREF2_POS are then attenuated by a factor of 16 by R433/R434 and R435/R436 respectively, to produceVREF3_NEG and VREF3_POS.

Hence:-

IREF_POS = + REF1/15.10^{-3}

IREF_NEG = - REF1/15.10^{-3}

VREF2_POS = + REF1/4

VREF2_NEG = - REF1/4

VREF3_POS = + REF1/64

VREF3_NEG = - REF1/64

IREF_POS and IREF_NEG are injected directly into the virtual earth point (Q5053) of the integrator, where they inject a current equivalent to voltage REF1 operating into an input resistance of 15kΩ.

Because reference voltages VREF2_POS/_NEG and VREF3_POS/_NEG operate into an input resistance of 60kΩ (R41610-7/5-12/14-3/1-16) they only have on quarter the weighting of IREF_POS and IREF_NEG.

Hence at the virtual earth point of the integrator:-

IREF_POS ≡ + REF1

IREF_NEG ≡ - REF1

VREF2_POS ≡ + REF1/16

VREF2_NEG ≡ - REF1/16

VREF3_POS ≡ + REF1/256

VREF3_NEG ≡ - REF1/256

5.2.5.1 Secondary Reference

The 4920M contains a 6.95V secondary reference, U402, which is used during the instrument's self-test routines to check the A-D converter's performance.

5.2.6 Digital PCB

(Circuit Diagram DC400933 Sheets 1 to 6; Pages 11.3-1 to 11.3-7)

5.2.6.1 Functional Block Diagram

Fig. 5.2.6.1 shows the main groups of functional circuits on the Digital PCB.

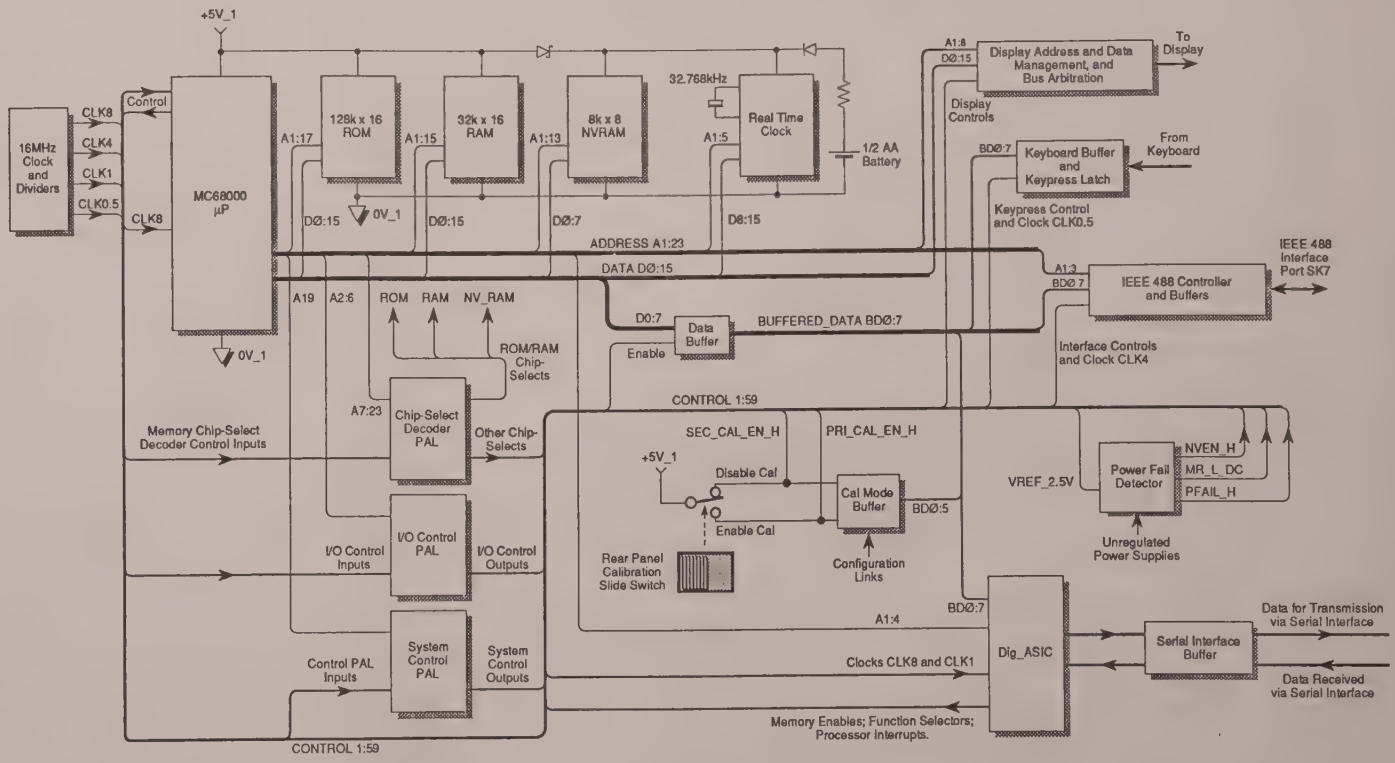


FIG. 5.2.6.1 DIGITAL PCB - BLOCK DIAGRAM

5.2.6.2 Processing, Memory and Organization

Clocks

All synchronizing clocks used on the Digital PCB are derived from 16MHz crystal oscillator Y101. Four clocks are required; produced by division in U101:

CLK8: 8MHz for the Processor and Digital ASIC.
CLK4: 4MHz for the IEEE 488 I/F Controller.
CLK1: 1MHz for the Digital ASIC.
CLK0.5: 500kHz for the Display Controller.

Processor

The instrument is internally controlled by 68000-series microprocessor U102. It translates all information, from the front panel keys and IEEE 488 interface, into control signals which determine the instrument's operation.

Data Transfers

Normal data transfers are processed via all address lines A1-A23 (Address Bus) and all data lines DØ-D15 (Data Bus), using the 68000's word and byte divisions and strobes. Other control signals in and out of the processor are grouped in the circuit diagrams as a 'Control Bus', but this is merely for clarity — the lines are in practice distributed on the PCB.

Different devices need different access times, and the processor requires read/write cycles to be terminated by handshaking signals in order to achieve maximum operating speed. The instrument accomodates three different access times:

250ns:	Normal RAM, EPROM, ASIC and Interrupt Acknowledge.
500ns:	IEEE 488 Controller, NV RAM, and Display.
1µs:	Switch status buffers.

Memory Assignment

EPROMs U103 and U104 hold 256kbytes of 16-bit program code and fixed data. U112 and U105 provide 64kbytes of 16-bit wide workspace RAM.

U106 is a low-power 8kbyte static RAM which is permanently powered — either by the +5V supply when the 4920M is powered from a line supply, or by 2/3 AA battery BT1 when the instrument is switched off. This 'non-volatile' memory contains calibration constants which are stored during instrument calibration, and subsequently used to correct readings during normal operation.

Memory Access

The EPROM chips are device-enabled by the Decoder PAL U110 from addresses A20-A23. U103 and U104 are chip-enabled together by A19, and addressed via lines A1-A17. Data bytes are read in parallel by simultaneous addressing; U103 outputs the 'upper' byte onto data bus lines D8-D15, and the 'lower' byte is read from U104 onto DØ-D7.

The workspace RAM chips are selected by the Decoder PAL U110, and addressed via lines A1-A15. Data bytes are read in parallel by simultaneous addressing. For RAM data, U112 contains by the 'upper' byte D8-D15 and U105 contains the 'lower' byte DØ-D7. Device-enable and read-write are selected via the control bus.

The non-volatile RAM U106 is also selected by the Decoder PAL U110, and addressed via lines A1-A14. For non-volatile RAM data, U106 contains the 'lower' byte DØ-D7. Device-enable and read-write are selected via the control bus, and write operations are inhibited unless calibration is enabled. The NV RAM is divided into three areas:

1. Primary Calibration Constants (External Calibration);
2. Special Calibration Constants (Factory Calibration);
3. User NV (Password, Bus Address etc.).

The Primary Calibration Constant and Special Calibration Constant areas are protected against unauthorised Write access by the rear panel Cal/Run switch. User NV, by necessity, is not switch protected.

Control Decoding

Three PALs: U107, U110 and U111, manipulate the various signals which are used to control instrument operation. Generally, U110 deals mainly with memory selection and calibration processes; the inputs to U111 are decoded to select devices other than memory. U107 operates mainly on handshake signals to and from devices which require longer access times.

Buffered Data Bus

The lower data bus byte DØ-D7 is connected to the two-way buffer U201 to provide the Buffered Data Bus BDØ-BD7. This is used to access several devices: Keyboard, Cal Mode Buffer, Digital ASIC, IEEE 488 Interface Controller and the I/O Port. U201 is enabled by EN_BUF_L, and its direction is controlled by signal BR_HW_L.

5.2.6.3 Digital ASIC

The Digital ASIC U203 is a support chip designed specially for use in Datron's digital multimeters. It interfaces via 16 read-write registers and an interrupt handler.

Functions

1. 68000 bus time-out for one or more wait state pairs (DTACK). Bus error generation on invalid address time-out (BERR).
2. 68000 reset power delay PFAIL to RESET.
3. Programmable timer — 1 to 256ms with end-of-period interrupt output.
4. Tick interrupt — 10ms or 100ms period.
5. Internal counter — free-running for internal triggers 0s to 10s: 10-bit with selectable prescaling (10µs; 100µs; 1ms and 10ms). Software triggers are used for delays greater than 10 seconds.
6. Delay counter — one-shot to delay the start of an A-D conversion by 0 to 10s after a trigger: 10-bit with selectable prescaling (10µs; 100µs; 1ms and 10ms). Software delays are used for intervals greater than 10 seconds.
7. Serial Interface - two-way communication between the 68000 and the Analog Sub-System.
8. Measurement time-out interrupt if the A-D converter locks up.
9. Write enable for non-volatile memory; and lockout circuit to detect illegal access.
10. Trigger conditioning:

    GET from IEEE 488 interface or front panel SAMPLE key.
    TRIG from rear panel BNC socket.
    Internal interval counter.

11. 68000 interrupt handler - interrupts from serial interface, triggers and external pins (NMI; GPIA; ERR; FPINT; RTCINT).

5.2.6.4 Conversion Initiate (CI_R)

Triggers

Firmware determines the way triggers are treated in the digital ASIC trigger conditioning circuit. Triggers may be disabled, cause an interrupt, or produce CI_R depending on conditions. The maximum rate at which the analog sub-system can respond to CI_R's is determined by the A-D converter and the need to collect measurement information via the serial interface between triggers. The four trigger sources are:

Internal: Interval Counter - Hardware or Software
External: TRIG_F - rear Trigger BNC connector.
GET_R - from the IEEE bus.
SAMPLE - from the Front Panel key

A timer in the digital ASIC produces CI_R (20-40 CLK1 periods) after the various triggers.

Internal triggers are generated by the Interval Counter in the digital ASIC at a rate controlled over the data bus by the processor. Where the trigger period is less than 10 seconds a programmable free running counter produces 'direct' triggers at a rate set by the processor. For trigger intervals greater than 10 seconds, 'indirect' triggers are produced by software in response to RTX_R.

External triggers are conditioned; the conditioned triggers causing either an 'immediate' or 'delayed' trigger or an interrupt, depending on the configuration set by the processor. In the case of an interrupt, the trigger is eventually produced from the interval counter via software.

If the interval between two external triggers is too short, the second is stored and acted upon at the earliest opportunity. If repetitive external triggers occur above the maximum rate allowed by the set configuration, triggering continues at the maximum possible rate.

In summary, triggering includes the following features:

1. Internal triggers - Interval counter:
   Hardware: < 10 Seconds
   Software: > 10 Seconds
2. External triggers - Software
3. Direct triggers come from hardware.
4. Indirect triggers come from software.
5. Delayed triggers pass through the Delay Counter (max 10s delay).
6. Immediate triggers by-pass the Delay Counter.

The rear Trigger input is a BNC connector on the rear panel.

5.2.6.5 Display Management

(Circuit Diagram DC400933 Sheet 3; Page 11.3-4)

Data to be displayed on the front panel is stored in workspace RAM. The processor employs 'Bus Arbitration' so that the Display Management System can gain access to this information.

Display Data Access

When Display Management requires data, it asserts BR_L (Bus Request). In reply, the processor asserts BG_L (Bus Grant) to indicate that control of the bus will be released at the end of the current processor cycle. The end of the cycle is signalled to each of the control PALs by AS_L being cleared, which is decoded with BG_L by U107 (System Control PAL) as ST_BG_L.

This signal causes the Display Management system to take control, which it acknowledges by asserting BGACK_L (Bus Grant Acknowledge).

Display Management now has control of the bus. Signal DMA_L (Direct Memory Access) enables the RAM, and data is extracted using the Address and Data buses. Control of the bus is returned to the processor when BGACK_L is cleared.

Anode Data

DSHFT_R clocks anode data into the display's 100-bit serial register *(page 11.2-1)* as seven 16-bit words via DDATA_H. DLTCH_H latches this pattern when the next pattern is shifted in. The display is scanned by walking a Logic-1 along the 20-bit grid register, one step for each 7-word set of anode data. The Logic-1 is clocked by DLTCH_H.

DDATA_H

U309 and U310 form a 16-bit serial-in/parallel-out register to provide the serial data stream DDATA_H.

RAM Addressing

U304 is a +16 counter whose output DMA_REQ_H signals completion of each word to U305 and the Bus Arbitration System. U305 divides by seven and provides a word count for RAM addressing on WRDØ, WRD1 and WRD2.

The output from the ÷20 counter U306/U307 is a character (grid) count used for RAM addressing via octal buffer U303.

The divide-by-16 counter U304 is clocked by CLK0.5 through U302$_8$, U311$_4$ and U308$_4$. At the count of 15 the carry out bit U304$_{15}$ goes high setting DMA_REQ_H at U312$_{12}$. On the next edge of CLK0.5, BR_L is set at U312$_8$ to request bus control. While BR_L is set, the CLK0.5 input is disabled by U313/U302 and all counting and shifting is stopped.

The processor asserts BG_L but ST_BG_H stays low until AS_L is cleared. When AS_L goes high at the end of the processor cycle, ST_BG_H goes high and U313$_6$ is clocked low by CLK8 to assert BGACK_L.

As well as being the response to BG_L, BGACK_L provides an enable for the parallel-in/serial-out Display Data Shift Registers U309/U310.

CLK0.5 remains inhibited, now via U313$_5$, U311$_1$ to U302$_{12}$. U313$_5$ also sets U313$_{12}$ high, and on the next CLK8, DMA_L is set at U313$_8$. This clears BR_L.

DMA_L enables RAM U112 and U105 via SEL_RAM_L from U110$_{19}$ *(page 11.3-2)*. DMA_L also enables the address buffer U303, so the address set by WRDØ-WRD2 and CHRØ-CHR4 is applied to the address bus. The first of the seven anode data words is thus loaded into U309/U310 via the data bus.

In reponse to BGACK_L the processor clears BG_L, and hence ST_BG_H.

U313$_9$ going low removes the inhibit on CLK0.5 at U302$_{12}$, causes DMA_L to be cleared at U313$_8$, and thus removes the enable on address buffer U303.

DSHFT_R is produced from CLK0.5 via U302$_8$, U308$_4$ and U311$_{10}$. Sixteen edges of DSHFT_R load the U309/U310 data word into the display anodes serial register. The series of sixteen CLK0.5 clocks also produces another DMA_REQ_H at U304$_{15}$, so the DMA cycle is repeated.

U305 counts DMA_REQ_H to generate the seven-word count, U305$_{15}$ incrementing the character counter U306/U307 after each seven words, latching the pattern on the Front Panel. This causes the Logic-1 in the display grid register to be shifted to the next grid by DLTCH_H via U308$_{12}$.

WRD1, WRD2 and CLK0.5 are gated by U207$_{11}$ and U312$_5$ to produce DBLK_H which blanks the display while the last two of each group of seven words are being loaded.

DG20_H is produced at U308$_8$ from U307$_{15}$ after each set of 20 characters (140 words) to load a Logic-1 into the display grid register.

After a system reset, the display is blanked for approx. 500ms by R306/C302 to allow the RAM to be re-initialized by the processor; and to allow the display registers to synchronize with the Display Management address counters.

Display scan is inhibited by the action of DBLK_H in the display circuit.

The facility for display blanking by DOFF_H is not used in the 4920M. DOFF_H is cleared by the processor via the data bus and U208$_{19}$ *(page 11.3-3)* at power up reset.

5.2.6.6 Keyboard Interrupt

(Circuit Diagram DC400933 Sheet 3; Page 11.3-4)

KB5 from the keyboard encoder sets the Key Press Latch by clocking U3023. This signals FP_INT_L to the digital ASIC interrupt Handler at U20339 *(page 11.3-3.)*

The digital ASIC sets the interrupt level '2' on IPL1 and IPL0/2 (U20340 and U20341respectively *(page 11.3-3)* to indicate an interrupt to the processor.

The processor compares the interrupt level with its internal mask. Assuming that the interrupt is of higher priority, the processor completes the current instruction then sets its mask at level 2.

The processor then sets the interrupt level 2 on A1-A3, asserts AS_L and sets R_H/W_L high. At the same time FC0_H, FC1_H and FC2_H are set, asserting IACK_L at U10719 *(page 11.3-2).*

R_H/W_L and AS_L with IACK_L at U2034, U20357 and U20358 respectively cause the digital ASIC to output the relevant exception number on BDØ-BD7. Access time-out is by U107 setting UIDTACK_L, which drives the processor via U11016.

The processor is now in an exception cycle. From ROM it fetches the exception vector indicated by the digital ASIC. The two vector words hold the first of a series of addresses which contain the instructions to read the front panel keys.
(Note: should an interrupt of higher level occur (such as ERR_L from the analog circuitry), the processor will terminate the read from the front panel.)

The processor places the 'Read Front Panel' address on the address bus. This is decoded to assert RDFP_L by the address decoder U111 at pin 19. RDFP_L carries out the following actions:

1. resets the Key Press Latch by U3021;
2. enables the Keyboard Buffer U301;
3. causes DTACK_L to be asserted after 500ns via the digital ASIC access timeout circuit.

The Keyboard Buffer places the encoded key number at KBØ-KB5 onto the buffered data bus BDØ-BD7. The two-way buffer U201 *(page 11.3-3)* has been enabled by AS_L (IACK.AS_L) and its direction has been set by R_H/W_L. The keyboard code is thus passed via DØ-D7 to the processor which takes appropriate action determined by the particular key which was pressed.

5.2.6.7 IEEE Interface

(Circuit Diagram DC400933 Sheet 3; Page 11.3-4)

The IEEE controller (GPIA) U401 is connected to the IEEE bus via the buffers U402 and U403. Data is passed to and from the GPIA on the buffered data bus. Note that BDØ connects to D7, BD1 to D6 etc.

The GPIA is addressed via A1-A3, and runs on CLK4 to maintain bus handshake speed. It is enabled by SEL GPIA_L, derived from U11118 *(page 11.3-2)* and read/write is selected by BR_HW_L from U10717. LWR_L from U1093 must also be asserted for the processor to be able to write to the GPIA.

When a valid Group Execute Trigger is received over the IEEE bus, it is transferred via the buffered data bus to U208 for decoding, then passes as GET_R from U20816 to the digital ASIC. If triggers are allowed, CI_R is produced to initiate a measurement. Interrupts generated at U4019 (GPIA_INT_L) are fed to the interrupt handler in the digital ASIC.

The buffers U402 and U403 are selected to Send or Receive by the GPIA U40121.

The GPIA has some internal de-bounce capability but extra provision has been made by fitting filter R401/C401 and R402/C402 to avoid problems which could arise due to external noise on IFC and REN.

5.2.7.4 Data and Control Lines

DOUT_H and DRET_H
The Digital ASIC is buffered from the opto-isolators on the A-D converter PCB by U404 *(page 11.3-5)*. From Fig.5.2.7.1 it can be seen that the data line loops around all the transmit/receive devices in the analog sub-system, entering via the opto-isolator U6032-7 on the A-D converter PCB as DOUT_H, and returning via U6042-7 as DRET_H.

SCLK_F (Transfer Clock)
Clock pulses on the SCLK_F line are fed to all transmit/receive devices through U6023-6 on the A-D converter PCB. Their purpose is to clock the data round the serial loop.

EN_H (Transfer Enable)
This signal goes high to enable data transfers around the loop. The condition of the serial data line during the first four SCLK_F pulses when EN_H is high determines the 'Receive/Send' state of the transmit/receive devices in the analog sections of the instrument. When EN_H is low, the transmit/receive devices are placed into 'WAIT' state.

TRK_H
This signal is not used.

ERR_L (Transfer Error Warning)
During a write cycle the transmit/receive devices compare the transmitted bytes of true data against the transmitted complement data. If there is any disparity, ERR_L is asserted. The ERR_L line remains high when there are no errors.

The ERR_L line can also be pulled low if a transmit/receive device does not recognize the bit-pattern of its received true data as a valid command, or if its internal processing is defective.

CI_R (Conversion Initiate)
This signal is used to initiate an A-D conversion. Once the correct trigger is present, the analog sub-system has been configured by data transfers, and any digital delays have expired, the CI_R line is set high. CI-R passes through opto-isolator U6033-6 and buffer U6066-14 on the A-D converter PCB becoming CI1-R and CI2-R. The rising edge of CI1-R into U509 on the A-D converter PCB initiates a reading conversion. At the same time, the frequency counter U606 on the High Accuracy AC PCB is activated.

RTX_R (Conversion and Count Complete)
The A-D converter control ASIC (U509 on the A-D converter PCB) has an open-collector output RTX, which is pulled low during a conversion as a result of CI_R. Once the conversion is completed the A-D converter control ASIC turns its open-collector RTX driver off, and RTX1-R goes high provided that the RTX output of the frequency counter IC is not holding it low.

Similarly the frequency counter (U606 on the High AccuracyAC PCB) has an open-collector output RTX, which CI_R causes to be pulled to low. Once the count is complete, the frequency counter turns its open-collector RTX driver off and RTX2-R goes high provided that the RTX output of the A-D converter control IC is not holding it low. When both the A-D converter control IC's and the frequency counter IC's RTX outputs have been released, pull-up resistor R6011-3 on the A-D Converter PCB pulls the RTX line high. This signal is passed through opto-isolator U6043-6 to the Digital ASIC, where the rising edge signifies that the two operations are finished.

5.2.7.5 WRITE Cycle

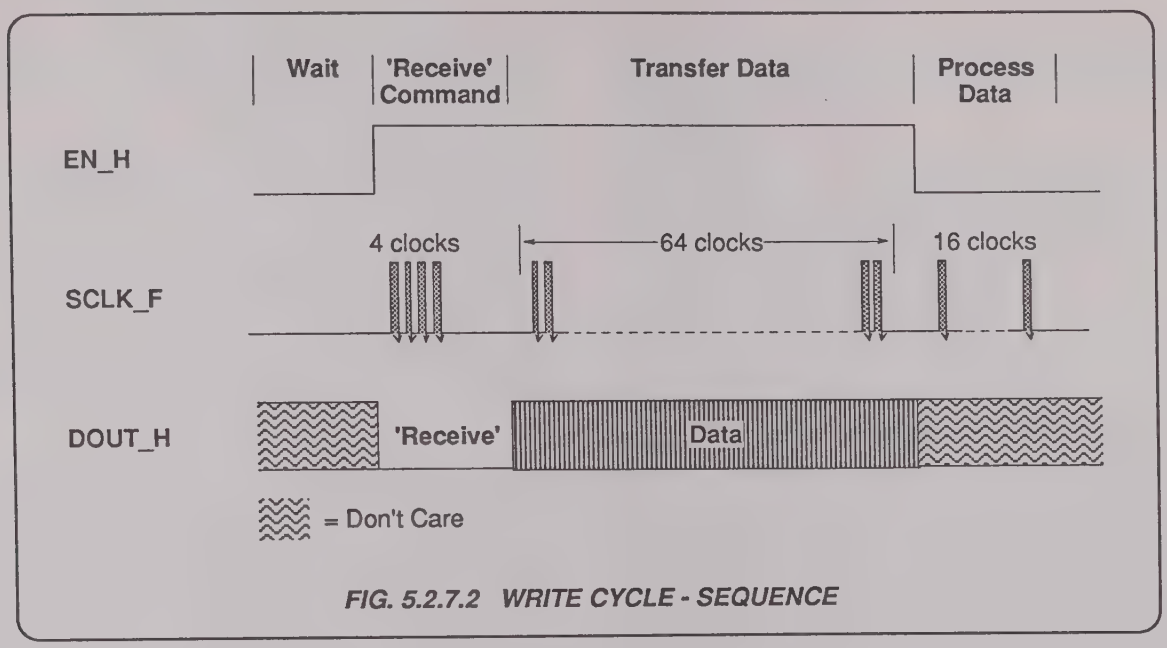


FIG. 5.2.7.2 WRITE CYCLE - SEQUENCE

There are four phases in the cycle, controlled by EN_H, SCLK_F and the data line DOUT_H itself. They are:

Wait:
EN_H is low, no clock pulses are present. All transmit/receive devices in the analog sub-system ignore data on the data line, effectively bypassing their serial registers.

Instruct All Transmit/Receive Devices to Receive:
EN_H goes high to enable the data transfer, and DOUT_H is set low. Four SCLK_F pulses are transmitted, while DOUT_H is held low, to announce that the processor is about to command a change of instrument analog state. The transmit/receive devices in the analog sub-system activate to receive data from DOUT_H, placing their serial registers into the data path. During the time taken to place the registers on line at the start of EN_H true, the inputs and outputs of the transmit/receive devices are still shorted, so the whole of the signal path has time to fall to a low state.

Transfer Data:
EN_H remains high. The 64 serial data bits of the first group are injected into the data path via DOUT_H, one bit at a time, while 64 SCLK_F pulses clock the bits through the serial registers of the transmit/receive devices. This transmission of 64-bit groups continues until the data is located in the appropriate transmit/receive serial registers. Each 8-bits of control information actually requires a 16-bit serial register in the data path – half for the true data byte, the other half for the complementary data byte which follows it. This allows error checking in the Process Data phase.

Process Data:
EN_H goes low to disable the data transfer. The data in the transmit/receive serial data registers is held, as the registers are taken out of the data path. Sixteen SCLK_F pulses are transmitted which cause the transmit/receive devices to check the true data against its the complemented data.

If there is no data corruption, the true control data is latched into the device's DIO lines (a similar checking facility is incorporated into the A-D converter control and frequency counter ASICs, but the correct true data is latched internally). The data is used to reconfigure the analog circuits that are controlled by the device.

If a device discovers an error, it pulls its ERR_L line low, and latches its DIO lines at high impedance. In this condition, a set of pull-up/pull-down resistors defines the state of the control lines to which the device is connected, setting them to a safe condition.

ERR_L operates is an open-collector output *and* as an input. When it is pulled low to indicate an error by one device, the change is detected by all the other devices in the loop, which also set their DIO lines to high impedance (but without latching). This causes the whole analog sub-system to revert to a safe condition.

There is a further benefit in latching only the device which detected the error. When fault-finding, if the transmit/receive chips are removed one at a time, then the ERR_L line will remain low until the one which reported the error is removed. This locates the part of the data stream which is corrupted, as a lead-in to subsequent fault diagnosis.

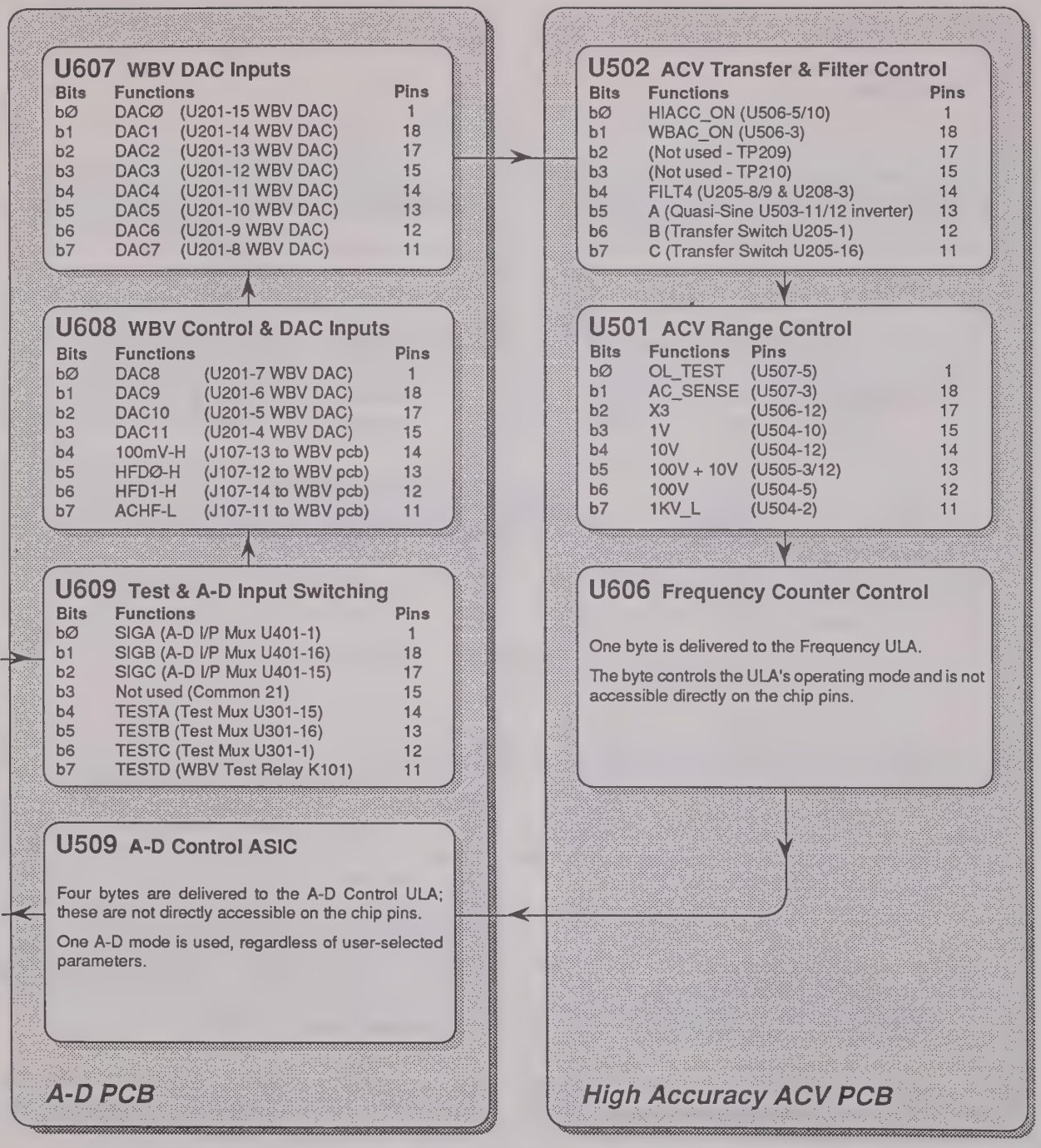

U607 WBV DAC Inputs
Bits Functions Pins
bØ DACØ (U201-15 WBV DAC) 1
b1 DAC1 (U201-14 WBV DAC) 18
b2 DAC2 (U201-13 WBV DAC) 17
b3 DAC3 (U201-12 WBV DAC) 15
b4 DAC4 (U201-11 WBV DAC) 14
b5 DAC5 (U201-10 WBV DAC) 13
b6 DAC6 (U201-9 WBV DAC) 12
b7 DAC7 (U201-8 WBV DAC) 11
U608 WBV Control & DAC Inputs
Bits Functions Pins
bØ DAC8 (U201-7 WBV DAC) 1
b1 DAC9 (U201-6 WBV DAC) 18
b2 DAC10 (U201-5 WBV DAC) 17
b3 DAC11 (U201-4 WBV DAC) 15
b4 100mV-H (J107-13 to WBV pcb) 14
b5 HFDØ-H (J107-12 to WBV pcb) 13
b6 HFD1-H (J107-14 to WBV pcb) 12
b7 ACHF-L (J107-11 to WBV pcb) 11
U609 Test & A-D Input Switching
Bits Functions Pins
bØ SIGA (A-D I/P Mux U401-1) 1
b1 SIGB (A-D I/P Mux U401-16) 18
b2 SIGC (A-D I/P Mux U401-15) 17
b3 Not used (Common 21) 15
b4 TESTA (Test Mux U301-15) 14
b5 TESTB (Test Mux U301-16) 13
b6 TESTC (Test Mux U301-1) 12
b7 TESTD (WBV Test Relay K101) 11
U509 A-D Control ASIC
Four bytes are delivered to the A-D Control ULA; these are not directly accessible on the chip pins.
One A-D mode is used, regardless of user-selected parameters.
A-D PCB
U502 ACV Transfer & Filter Control
Bits Functions Pins
bØ HIACC_ON (U506-5/10) 1
b1 WBAC_ON (U506-3) 18
b2 (Not used - TP209) 17
b3 (Not used - TP210) 15
b4 FILT4 (U205-8/9 & U208-3) 14
b5 A (Quasi-Sine U503-11/12 inverter) 13
b6 B (Transfer Switch U205-1) 12
b7 C (Transfer Switch U205-16) 11
U501 ACV Range Control
Bits Functions Pins
bØ OL_TEST (U507-5) 1
b1 AC_SENSE (U507-3) 18
b2 X3 (U506-12) 17
b3 1V (U504-10) 15
b4 10V (U504-12) 14
b5 100V + 10V (U505-3/12) 13
b6 100V (U504-5) 12
b7 1KV_L (U504-2) 11
U606 Frequency Counter Control
One byte is delivered to the Frequency ULA.
The byte controls the ULA's operating mode and is not accessible directly on the chip pins.
High Accuracy ACV PCB

FIG. 5.2.7.3 SERIAL INTERFACE REGISTERS - COMMAND DATA (DEVICES SET TO RECEIVE)

5.2.7.6 READ Cycle

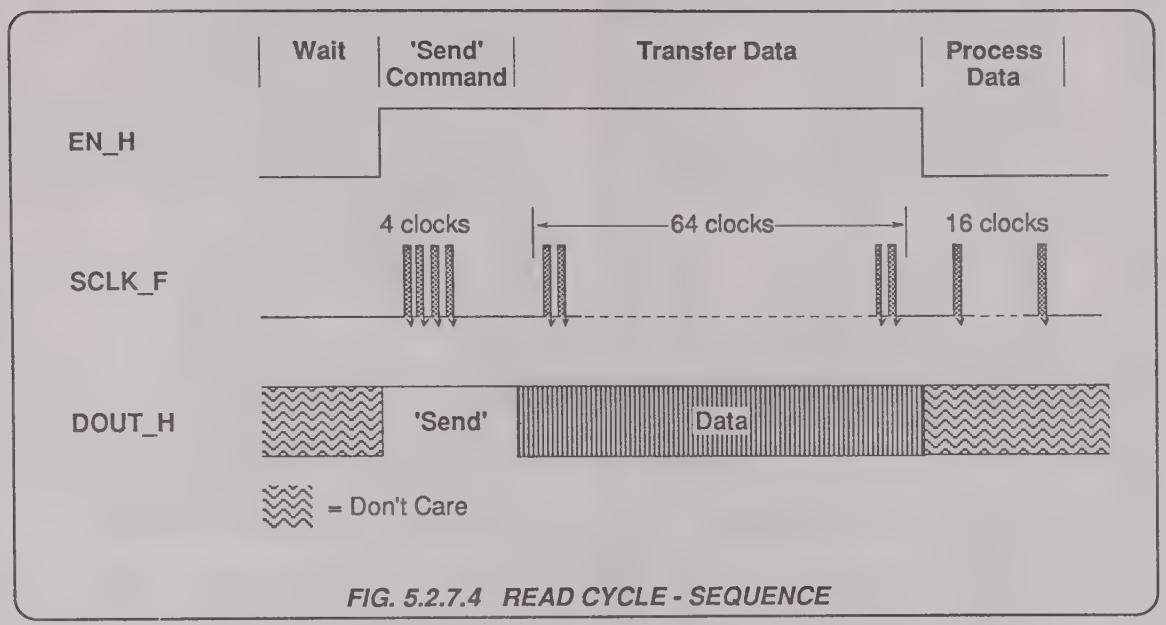


FIG. 5.2.7.4 READ CYCLE - SEQUENCE

There are four phases in the read cycle, also controlled by EN_H, SCLK_F and the data line DOUT_H. They are:

Wait:
EN_H is low, no clock pulses are present. All transmit/receive devices in the analog sub-system ignore any data on the data line, effectively bypassing their serial registers.

Instruct All Transmit/Receive Devices into their Preset Send Modes:
EN_H goes high to enable the data transfer. Four SCLK_F pulses are transmitted, while DOUT_H is held high, to announce that the processor is about to command the 'Send' devices to transmit data. The 8-bit transmit/receive devices in the analog sub-system are preset in hardware as 'receiver only' and so assume the 'Wait' condition, in which they are transparent to signals on the serial data path. The A-D converter control and frequency counter ASICs activate to transmit data via DRET_H, placing their serial registers into the data path. During the time taken to place the registers on line at the start of EN_H true, the inputs and outputs of the transmit/receive devices are still shorted, so the whole of the signal path has time to rise to high state.

Transfer Data:
EN_H remains high. 64 preset serial data bits of the first group are injected into the data path via DOUT_H, a bit at a time, while 64 SCLK_F pulses clock the bits through the A-D converter control and frequency counter ASICs' serial registers. This transmission of 64-bit groups continues until the preset data is returned to the digital ASIC serial registers. The A/D converter control and frequency counter ASICs generate both true and complement data bytes to permit error checking by the digital ASIC during the Process Data phase.

Process Data:
EN_H goes low to disable the data transfer. The data in the transmit/receive serial data registers is held, as the registers are taken out of the data path. Sixteen SCLK_F pulses are transmitted which cause the A-D converter control and frequency counter ASICs to check their new received data against its complement, and at the same time the digital ASIC checks the returned true and complement data from the A-D converter control and frequency counter ASICs.

If there is no corruption, the returned true data is transferred to the 68000 microprocessor.

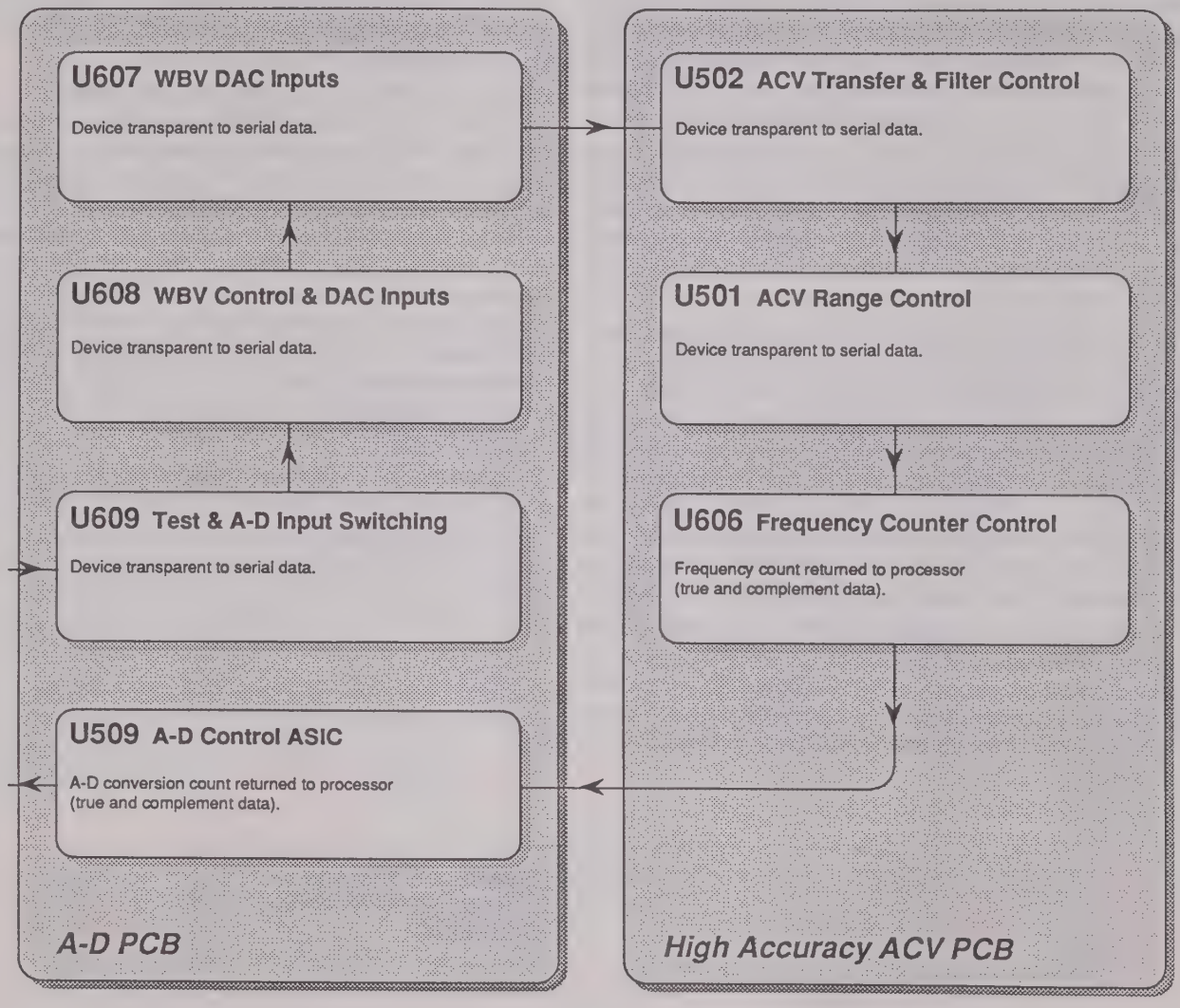

U607 WBV DAC Inputs
Device transparent to serial data.
U608 WBV Control & DAC Inputs
Device transparent to serial data.
U609 Test & A-D Input Switching
Device transparent to serial data.
U509 A-D Control ASIC
A-D conversion count returned to processor
(true and complement data).
A-D PCB
U502 ACV Transfer & Filter Control
Device transparent to serial data.
U501 ACV Range Control
Device transparent to serial data.
U606 Frequency Counter Control
Frequency count returned to processor
(true and complement data).
High Accuracy ACV PCB

FIG. 5.2.7.5 SERIAL INTERFACE REGISTERS - MEASUREMENT DATA (DEVICES SET TO SEND)

5.2.7.7 Internal Serial Interface Test

Introduction
This is one of the first commands from the processor to the Serial Interface Controller ASIC following a Reset (including a power-up reset). Its is included so that the processor can establish that the internal serial interface is fully functional, and that safe analog control signals can be established within the instrument.

The 8-bit transmit/receive devices have a hardware reset which configures them as receivers, but they are designed so that this reset state can be overridden when commanded via the serial interface. Once overridden, they can revert to 'receiver mode' only when the override is cancelled by a write cycle, or after a further reset.

The internal serial interface test command generates three transfers, overriding the hardware preset. The first two are abbreviated Read cycles, which command all transmit/receive devices (except the A-D converter control ASIC) to convert into 'Senders' and set their DIO lines at high impedance. The analog sub-system is thus configured safe by the pull-up/pull-down resistors on the DIO lines. This imposes a unique bit-pattern for each transmit/receive device, which is monitored by the device as an input from the DIO lines and is loaded (with its complement data) into the device's serial register in the interface data path.

The third transfer is a standard Read cycle, which passes the data from the transmit/receive devices to the digital control ASIC. After checking for errors, the digital control ASIC releases the data for the processor to read. The processor examines the bit patterns returned from the analog sub-system to check that they are correct.

Wait:
EN_H is low, no clock pulses are present. All transmit/receive devices in the analog sub-system ignore any data on the data line, effectively bypassing their serial registers.

Instruct Transmit/Receive Devices to Test Mode:
EN_H goes high. Four SCLK_F pulses are transmitted, while DOUT_H is held high. EN_H immediately returns to low, and 16 SCLK_F pulses are transmitted to clock the 'Process Data' sequence in the transmit/receive devices in the analog sub-system. Each transmit/receive device (except the A-D converter control ASIC) interprets this sequence as the overriding 'All Send Interface Test Data' command. Each one reconfigures itself as a sender, setting its DIO lines at high impedance and loading the DIO bit-pattern into its serial register. During the time taken to place the registers on line at the start of EN_H true, the inputs and outputs of the transmit/receive devices are still shorted, so the whole of the signal path has time to rise to high.

To ensure that the transmit/receive devices have enough time to reconfigure themselves, the instruction is repeated a second time.

Instruct Transmit/Receive Devices to Send Data:
The processor commands a Read cycle to obtain the test data.

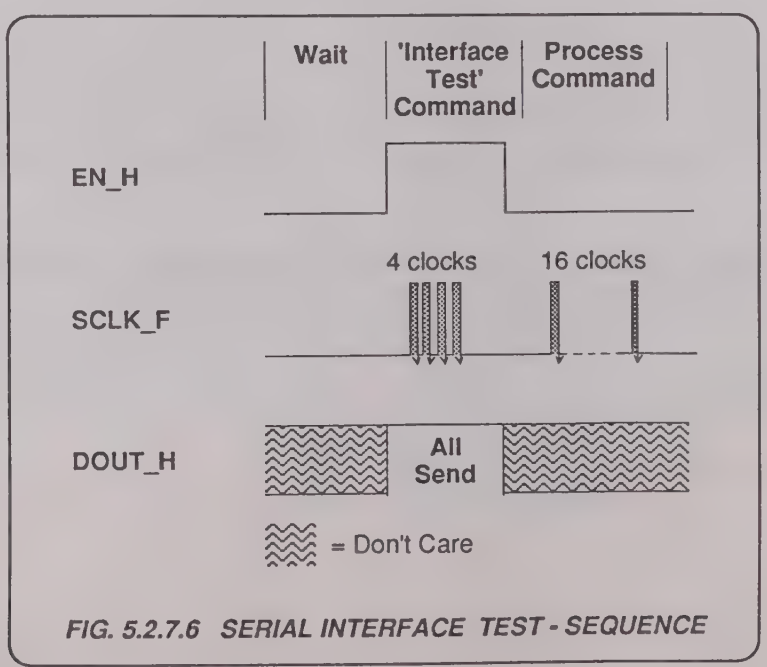


FIG. 5.2.7.6 SERIAL INTERFACE TEST - SEQUENCE

5.2.7.8 Power On and Reset

Interface Flushing

At power on, the digital master reset MR_L is asserted, to be turned off after 200ms-300ms. Because the transmit/receive devices in the analog sub-system could power up any random condition, they must be initialized. The first action by the processor on the interface is to flush the serial interface data path by 16 SCLK_F pulses, while DOUT_H and EN_H are held low. The transmit/receive devices are thus in the safe 'Wait' state, their DIO lines being at high impedance due to EN_H being low, serial data registers off-line, and serial data inputs and outputs shorted together. The 16 SCLK_F pulses are therefore sufficient to set the whole of the serial data path to low.

Interface Reset

Two Write cycles are processed with DOUT_H remaining low. This time the transmit/receive registers are put into the serial data path by EN_H high, and are all reset to zero by the low on the data path. This is a safe state, and after the reset the transmit/receive devices return to 'Wait' state.

Internal Serial Interface Test

Two internal serial interface test commands are transmitted to ensure that all transmit/recieve devices are forced to become senders, then a Read cycle is processed, using four 64-bit groups so that a complete test will be completed. If an interface error occurs at this time the processor will abort the test, deal with the error, and then re-start the test.

The transmit/receive devices remain in their 'Wait' condition, imposing the Power On Reset (default) condition on the analog sub-system, until a Write cycle is processed to change their serial register contents.

A-D Action

After the digital master reset has been removed, CI_R remains inactive until the internal serial interface test has been successfully completed, allowing the A-D converter control ASIC to stabilize the A-D converter's analog circuits. With 0V at its signal input, the A-D converter powers up with its integrator output positive, and the A-D converter control ASIC imposes +REF/256 to return this very slowly towards zero. Meanwhile, during the master reset period, the A-D converter control and frequency counter ASICs release their open-circuit RTX_R outputs, which remain pulled to a high state.

After the internal serial interface test has been completed successfully, a conversion is initiated by CI_R being set high for some 30ms. The rising edge of CI_R has the effect of imposing +REF at the A-D input, which rapidly drives the A-D output to zero, and the A-D starts a conversion with zero input. At the same time the RTX_R line is forced low. The processor waits for the RTX_R line to rise to high again to show that this first conversion has been completed. If this does not happen within 2.25 seconds, the processor assumes that an A-D converter fault is present.

A successful first conversion sets RTX_R back to high, and the interface power-on sequence is complete. Unless the instrument is commanded otherwise, the power-on default state persists, and the A-D converter is internally triggered.

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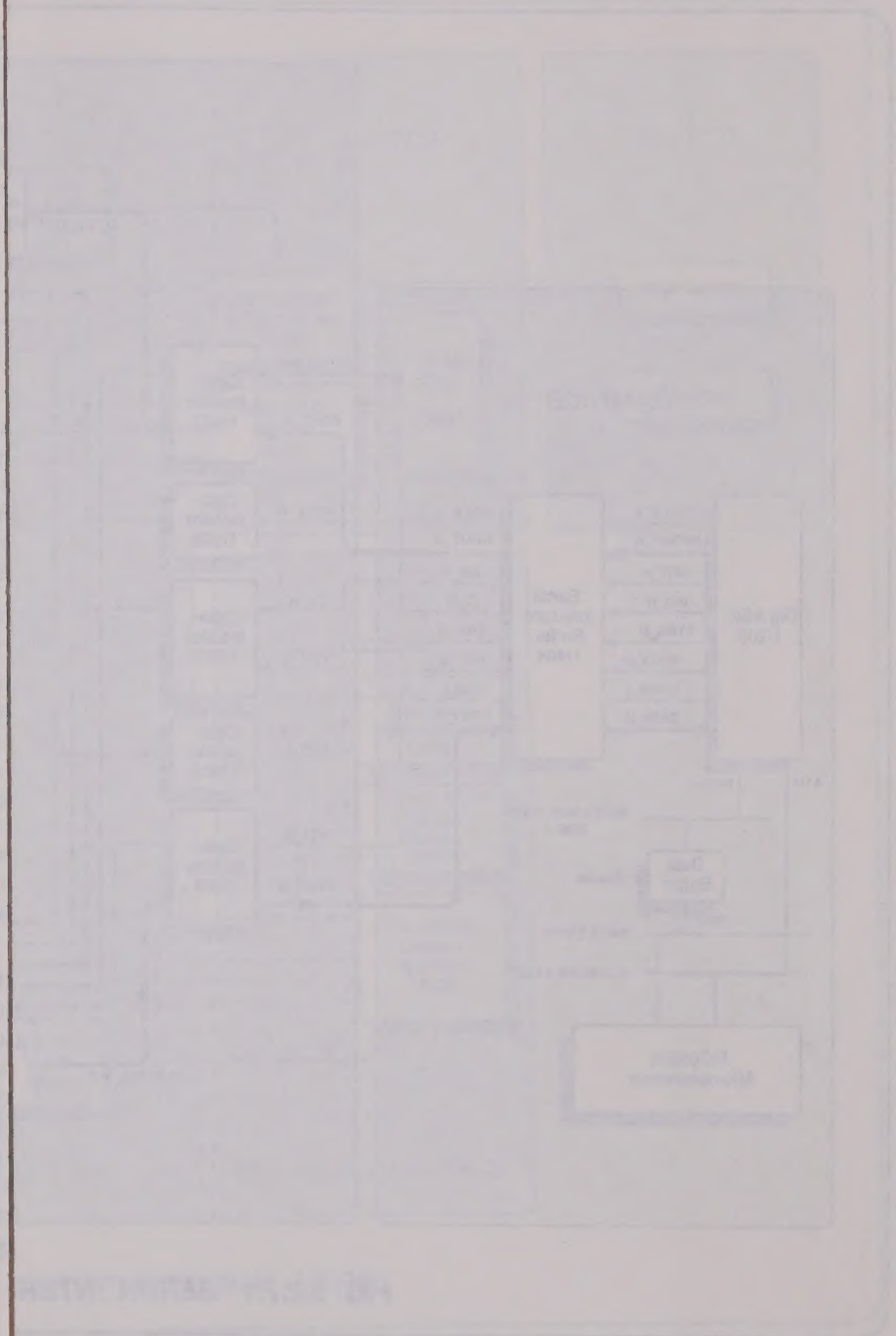

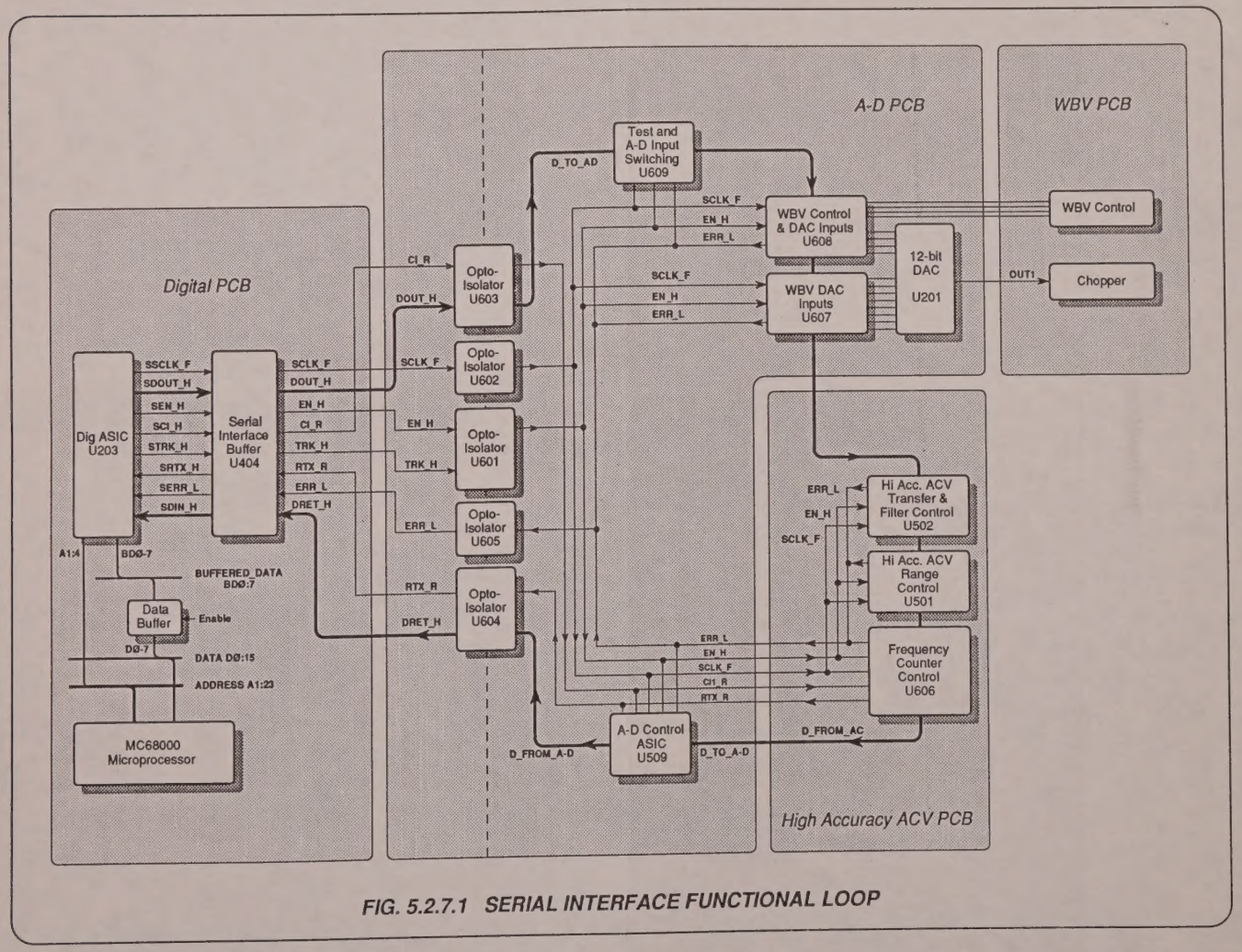

FIG. 5.2.7.1 SERIAL INTERFACE FUNCTIONAL LOOP

5.2.7 Serial Data interface

5.2.7.1 Functional Block Diagram

Fig. 5.2.7.1 (flyout) shows the elements and routing of the Serial Data Interface.

5.2.7.2 Need for a Serial Interface

If each of the analog control signals and analog status signals were to be passed between the digital control PCB and the analog PCBs via a dedicated latch/buffer, more than 50 latch/buffers would be required. Not only would this impose space penalties, it would also result in complex ground currents flowing between the digital and analog circuitry which could affect the 4920M's measurement performance.

By transferring all analog control and status information between the digital and analog sections of the 4920M via opto-islolators, ground current problems are eliminated. In addition, by transferring the information in the form of a bit-serial data stream, the total number of opto-isolators required is reduced to seven. This includes provision for two asynchronous signals (not directly connected with interface transfers) and three interface control signals.

5.2.7.3 Interface Control

Processor Control of the Interface

The Interface Controller is incorporated into the Digital ASIC U203 *(page 11.3-3)*. The 68000 processor controls the interface using A1-A4 and DBØ-DB7, together with address decodes SEL_ULA_L, LDS_L, R_HW_L and AS_L. Handshake signal UDTACK_L acknowledges when sufficient access time (250ns) has elapsed.

There are three main states of the interface:

WAIT: The interface is quiescent, awaiting instructions from the processor.

WRITE: The processor commands a change of instrument analog state via the interface.

READ: Status data is passed back to the processor from the analog circuits.

The processor instructs the Interface Controller to change the state of the interface by writing to the ASIC's command register over the buffered data bus BDØ-BD7. The controller can find out the interface state and any status information by reading the ASIC's status register via BDØ-BD7.

The Interface Controller can instruct the ASIC to request a processor interrupt via the IPLØ-IPL2 lines. When requested, the processor responds by returning the same priority level via the FCØ-FC2 lines. When the processor reaches the interface interrupt in the interrupt queue, it services it by setting IACK_L low at the ASIC. This acts as a chip-select, and the interrupt data is read back to the processor via the buffered data bus. As a result the processor carries out the next step in the write or read cycle.

Power-up and Reset

The ASIC is placed into Reset condition at power-up. When it is released from reset, the Interface Controller places the interface into the WAIT state. This causes all the transmit/receive devices in the analog sections of the instrument to take their serial registers off-line, and they become 'transparent' to any signals on the serial path. Effectively, they are in a bypassed condition.

From this point the processor controls the state of the interface, and via the interface, the instrument analog state.

Changing the Instrument Analog State

To do this the processor commands the interface state to WRITE and a write cycle begins. Control data to be transmitted via the interface is passed to the digital ASIC in 4-byte blocks over the buffered data bus. The digital ASIC assembles these blocks into 64-bit groups, each comprising four bytes of true data interlaced with four bytes of complement data. The true/complement data is then transmitted over the internal serial interface with transmit/receive devices in the analog sections of the instrument set to receive.

Obtaining Measurement and Status Information

To do this the processor commands the interface state to the READ mode and a read cycle begins. Read cycles are also initiated automatically when either the A-D converter or the frequency counter IC has generated new measurement data. The transmit/receive devices in the analog sections of the instrument are set to transmit, while receive only registers in the serial path become transparent. Measurement or status information to be returned from the A-D converter and frequency counter IC are loaded into their serial registers, and are transmitted to the digital ASIC.

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